I³N Innovative Integrated Instrumentation for Nanoscience

polifab POLITECNICO DI MILANO

POLITECNICO MILANO 1863

High Resolution Electronic Measurements in Nano-Bio Science

Measuring currents below 4K

Cryogenic electronics

Giorgio Ferrari

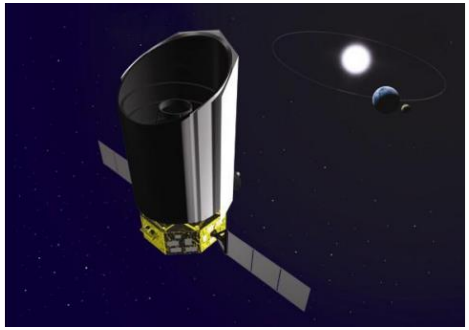
Milano, June 2023

Outline

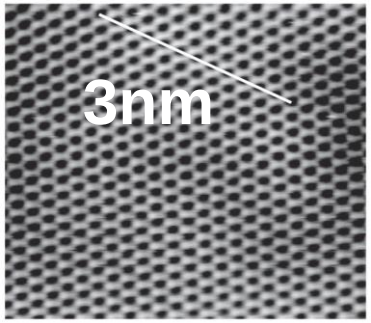
- Spin detection using room temperature instrumentation
- Cryogenic electronics
  - Challenges
  - Design rules
- Examples

Motivation for cryogenic electronics

- Space applications
  - $T_{deep\ space} \approx 3K$
  - mid- and far-infrared detectors require temperature below 5K



- Cryogenic STM/SPM systems
  - Less thermal fluctuations and drift

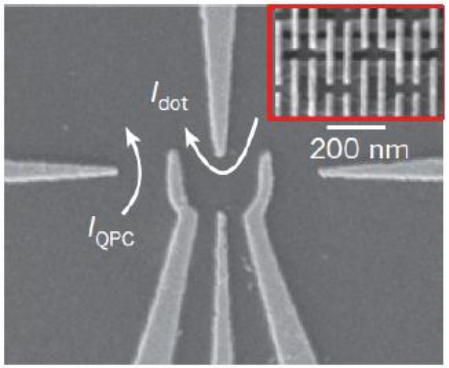


Rev. Sci. Instr., 121101 (2010)

graphene, profile ±20pm

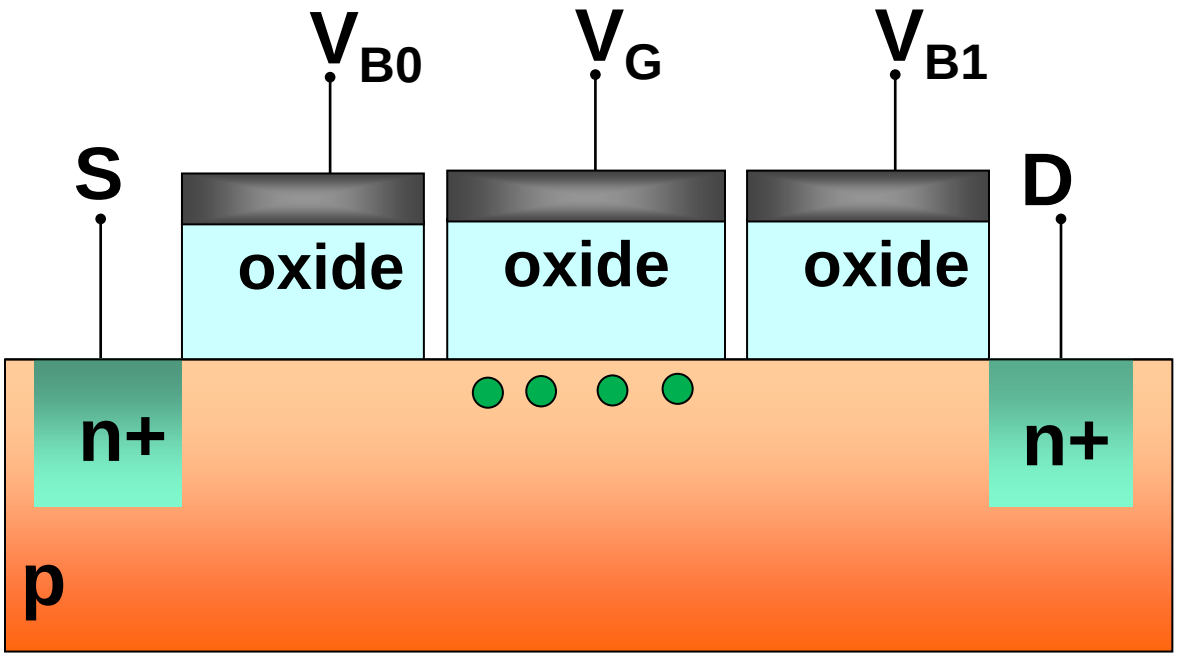
- Quantum devices and quantum computing
  - Low temperature for reducing thermal energy
  - Supercondutors

Readout and characterization of spin qubits



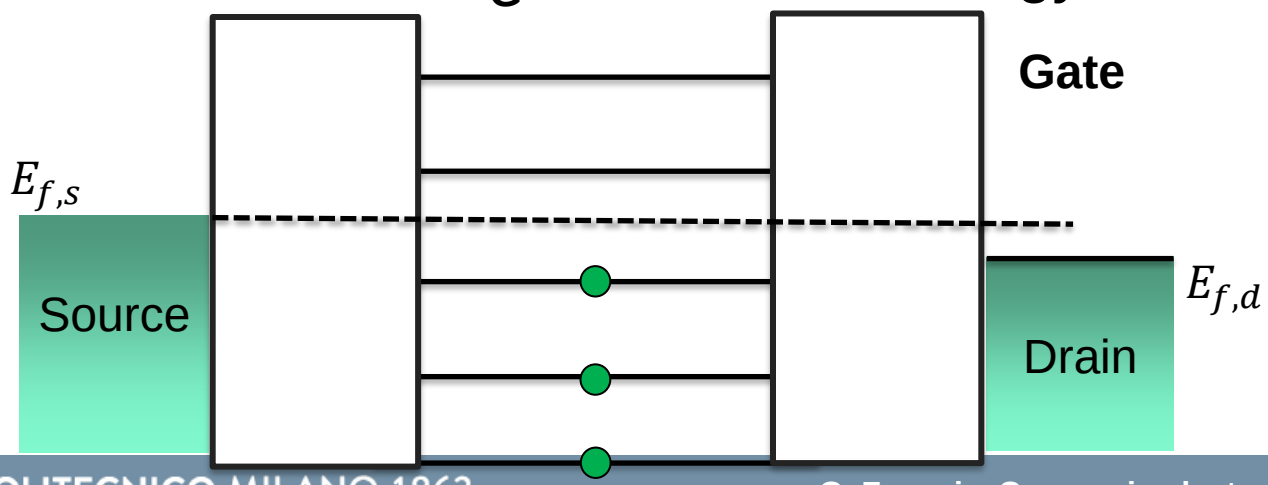
Nature 479, 345 (2011)

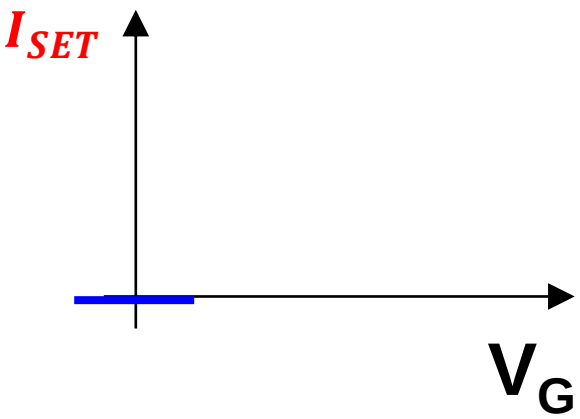
Single-Electron Transistor (SET)



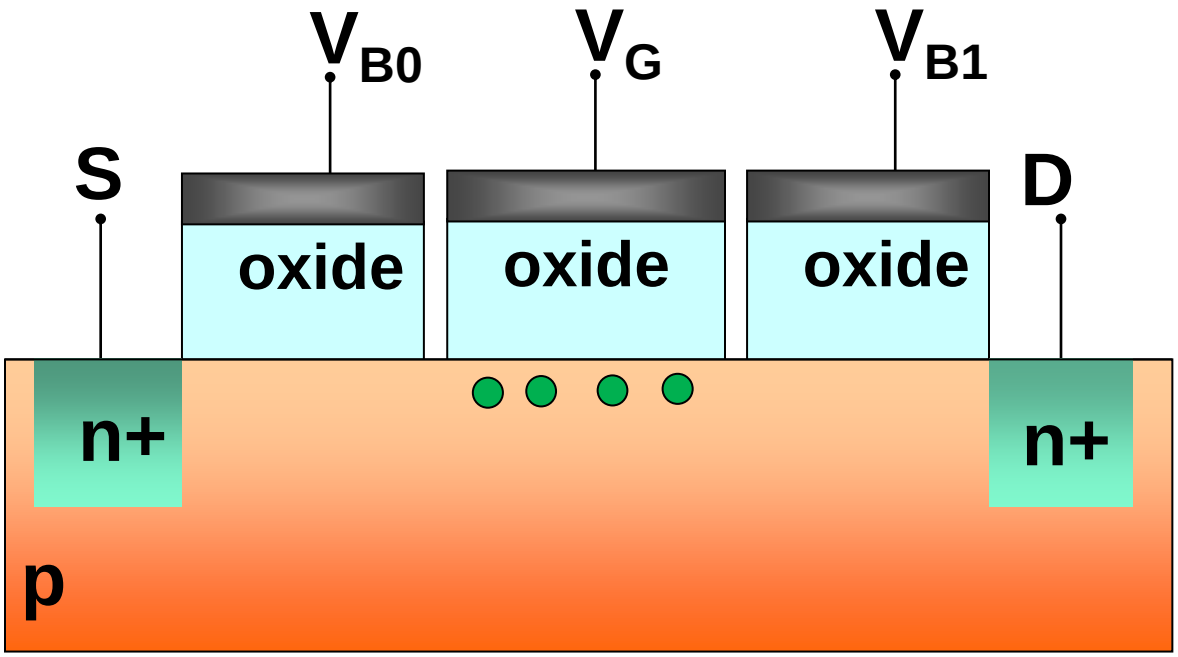
V_{B0}, V_{B1} biased to have an energy barrier for the electrons
The energy barrier is thin enough to allow tunneling

V_G controls the energy levels of the island

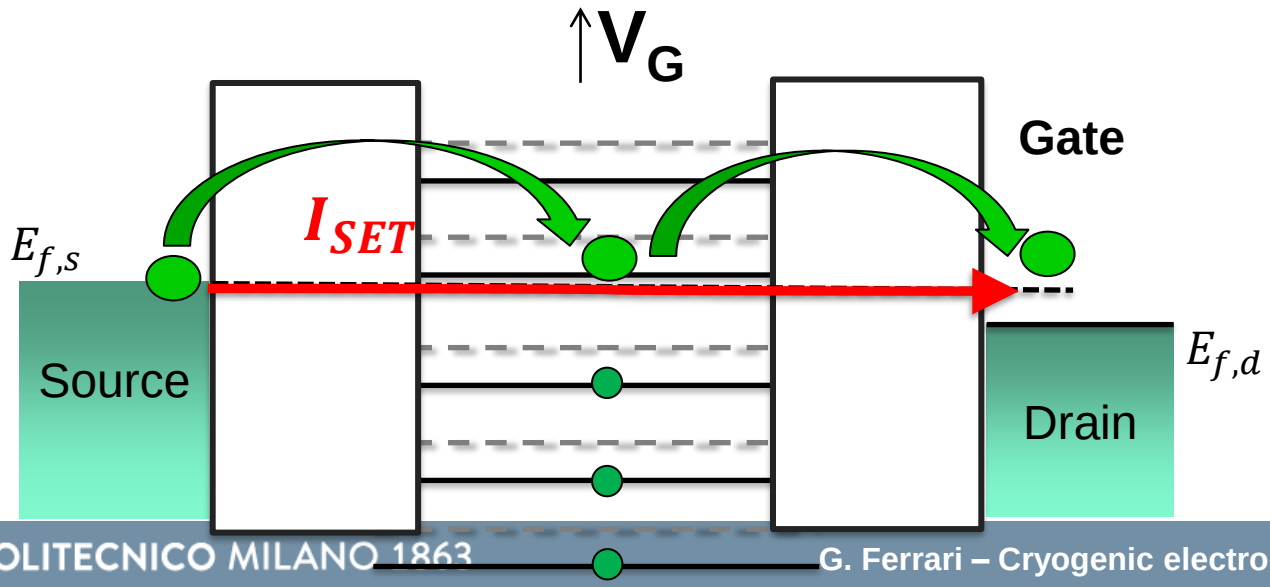


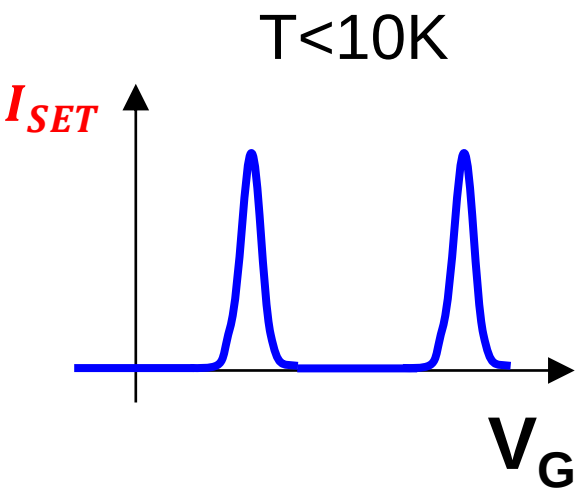


Single-Electron Transistor (SET)



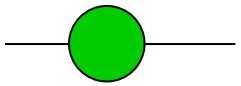
V_{B0}, V_{B1} biased to have an energy barrier for the electrons
The energy barrier is thin enough to allow tunneling





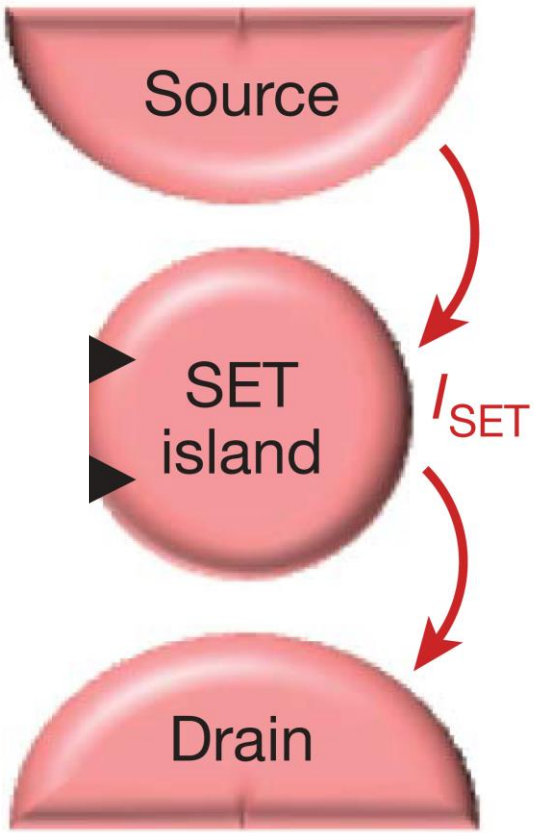
SET-based single-charge detector

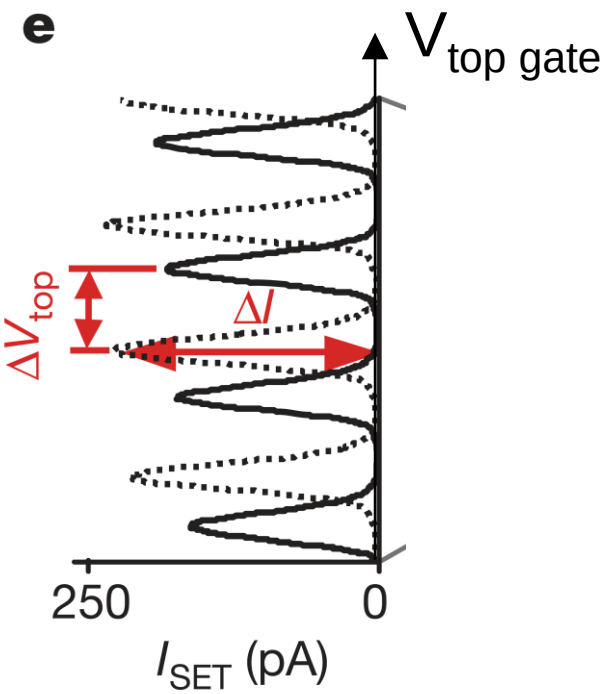
see Prati's lesson



Single electron

(donor)



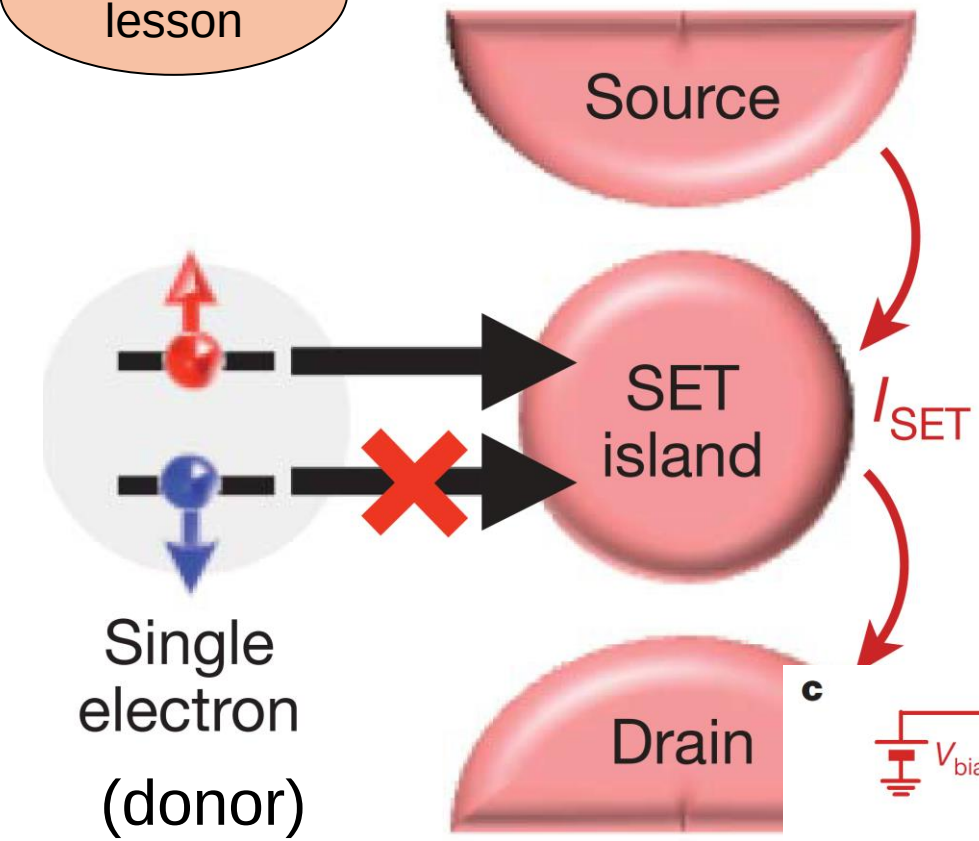


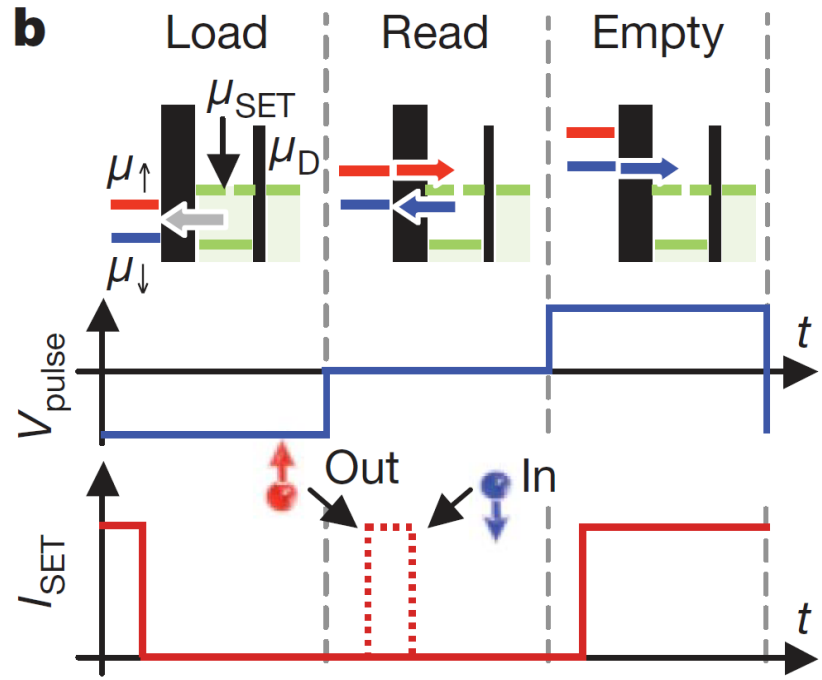
ΔV_{top}: voltage shift of the SET island given by the charge state of the donor

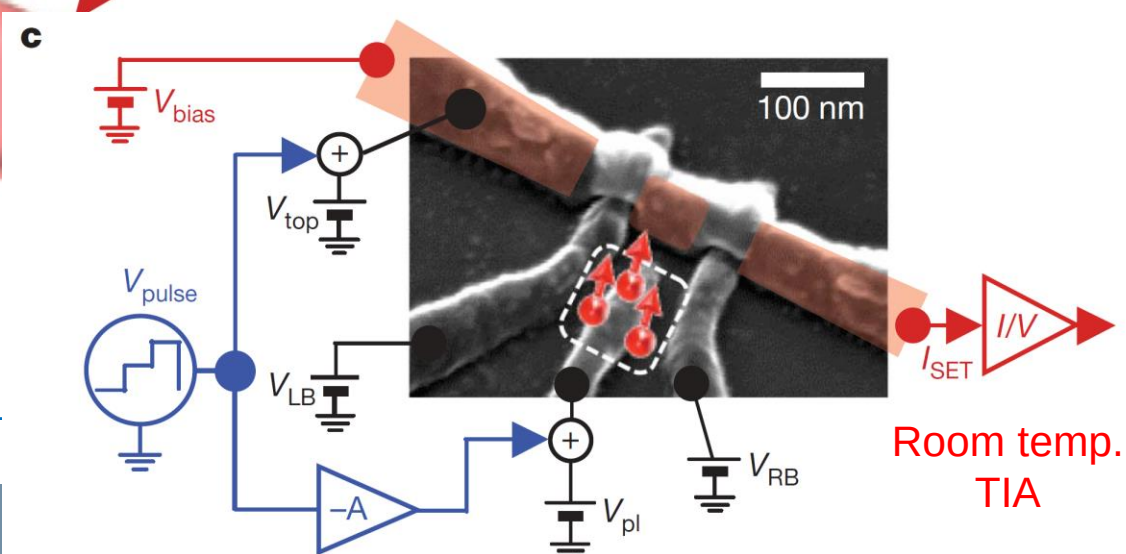
A. Morello,et al. *Nature*, no. 7316, pp. 687–91, 2010, doi: 10.1038/nature09392.

Spin state detection: spin-to-charge conversion

see Prati's lesson



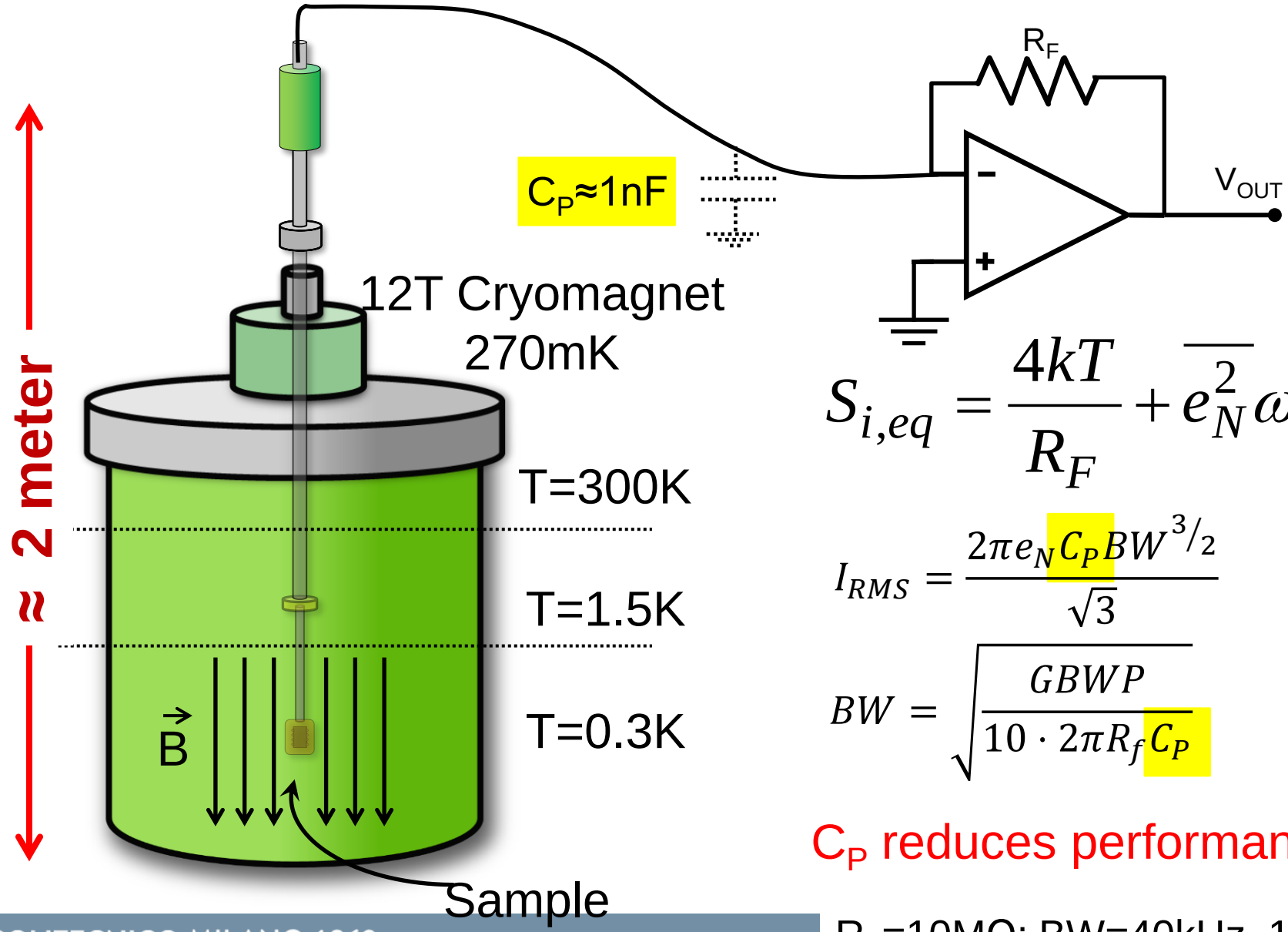




Room temp. TIA

A. Morello,et al. *Nature*, no. 7316, pp. 687–91 2010, doi: 10.1038/nature09392.

Experimental set-up to study quantum devices



$$S_{i,eq} = \frac{4kT}{R_F} + \overline{e_N^2}\,\omega^2 C_P^2$$

$$I_{RMS} = \frac{2\pi e_N C_P BW^{3/2}}{\sqrt{3}}$$

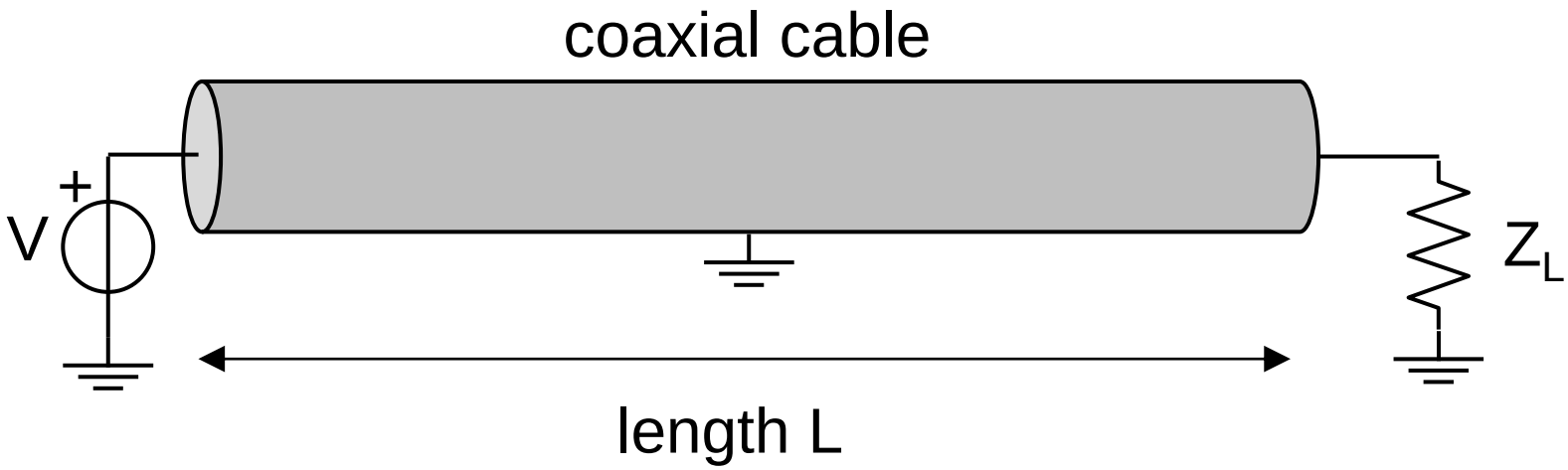
$$BW = \sqrt{\frac{GBWP}{10 \cdot 2\pi R_f C_P}}$$

C_P reduces performances

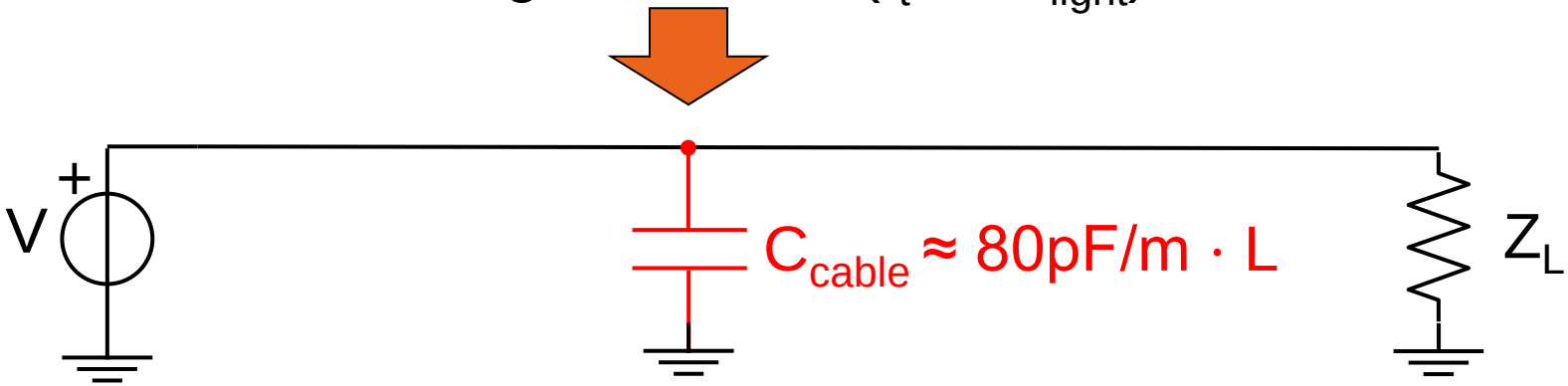
R_F=10MΩ: BW=40kHz, 150pArms

How to avoid being penalized by a long cable?

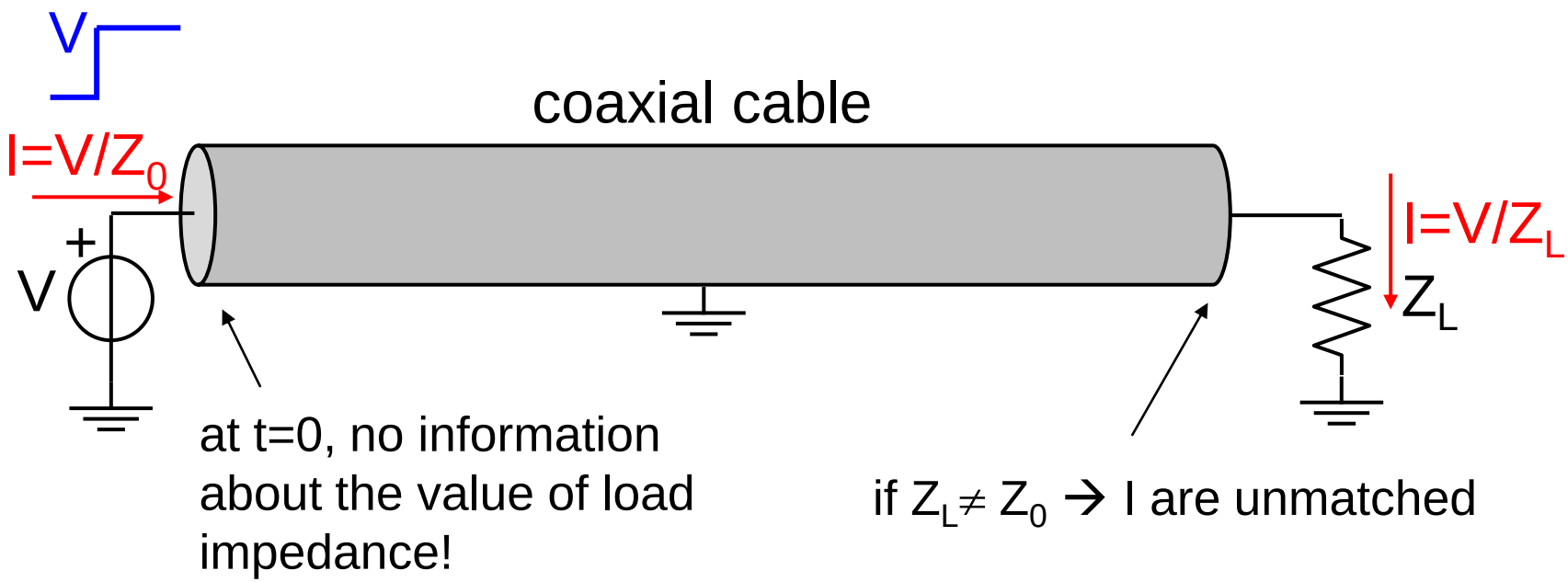
Measuring an impedance using the properties of the cable:



If V changes slowly compared to the transit time of the electromagnetic wave ($t_t = L/v_{light}$):

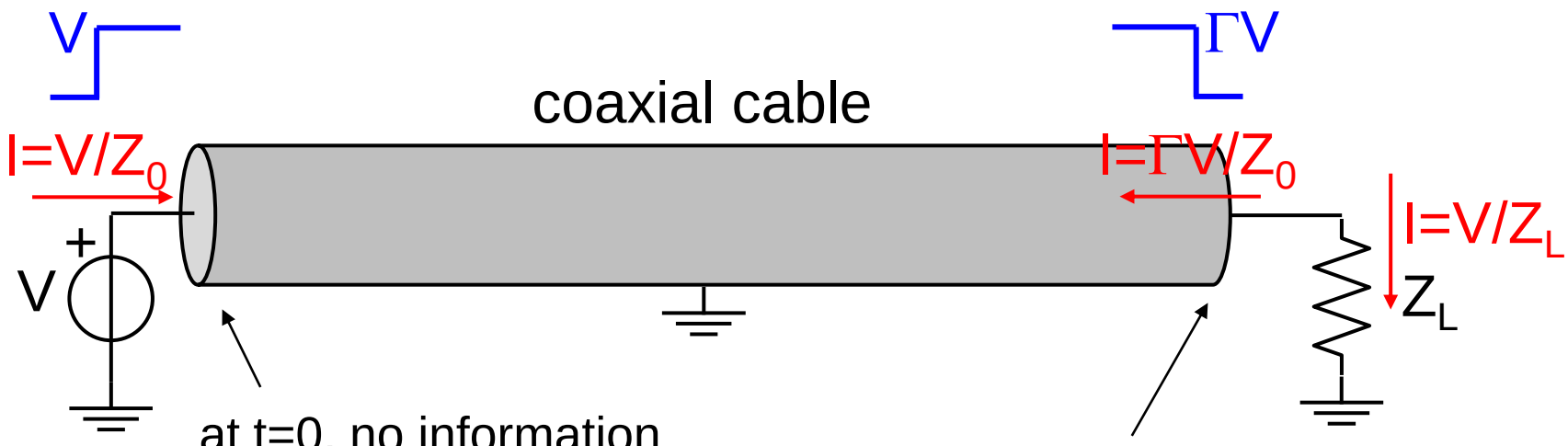


Transmission line



Z_0 = characteristic impedance of the cable, usually 50Ω

Transmission line



at t=0, no information on the load impedance!

if $Z_L \neq Z_0$ → I are unmatched

a reflected wave is created!

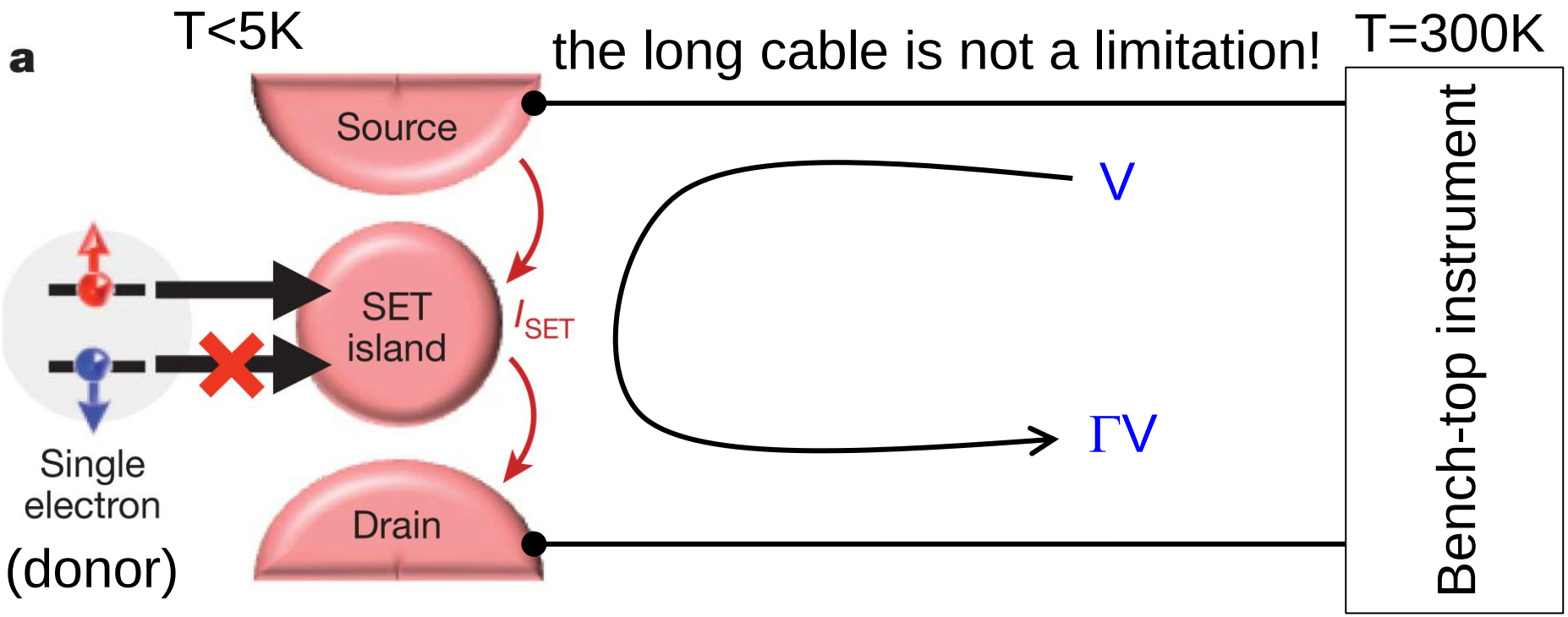
Z_0 = characteristic cable impedance, usually 50Ω

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}$$

reflection coefficient

The reflected wave is related to the load impedance!

Radio-frequency spin readout

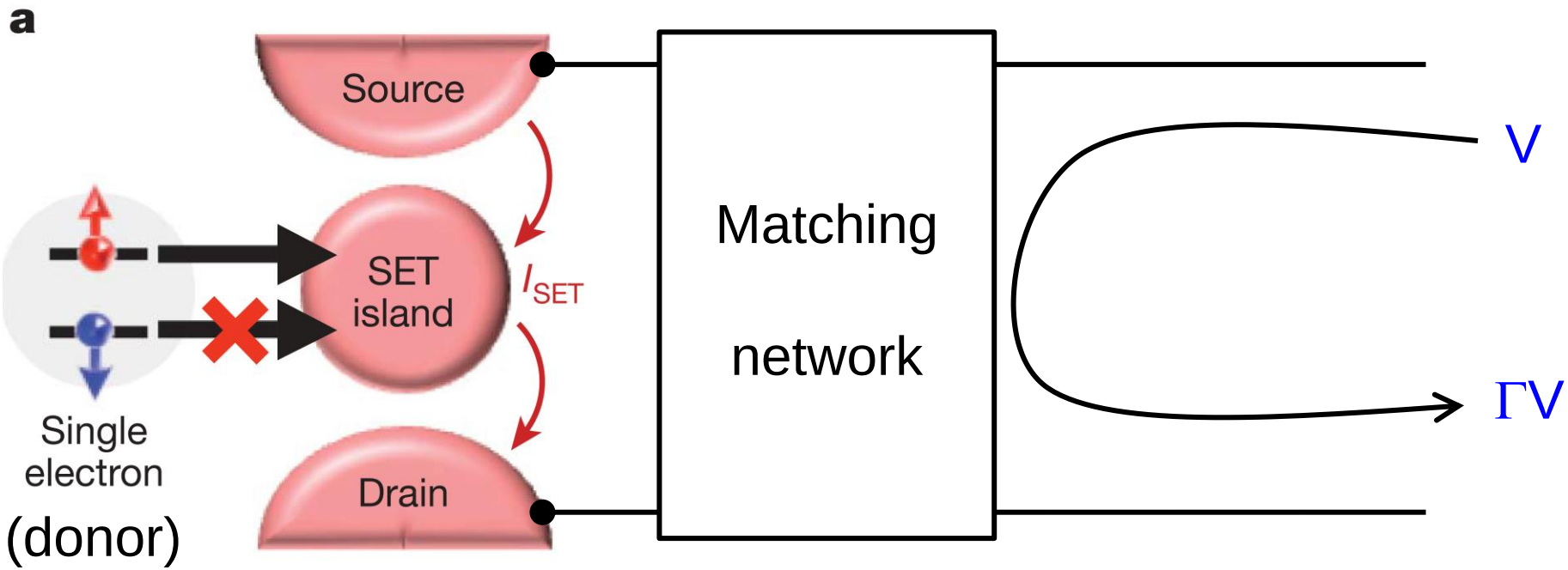


SET resistance depends on the donor charge that, in turn, depends on the spin

$$\Gamma = \frac{R_{SET} - Z_0}{R_{SET} + Z_0}$$

However, R_{SET}>25kΩ, Z_0≈ 50Ω ➡ limited sensitivity

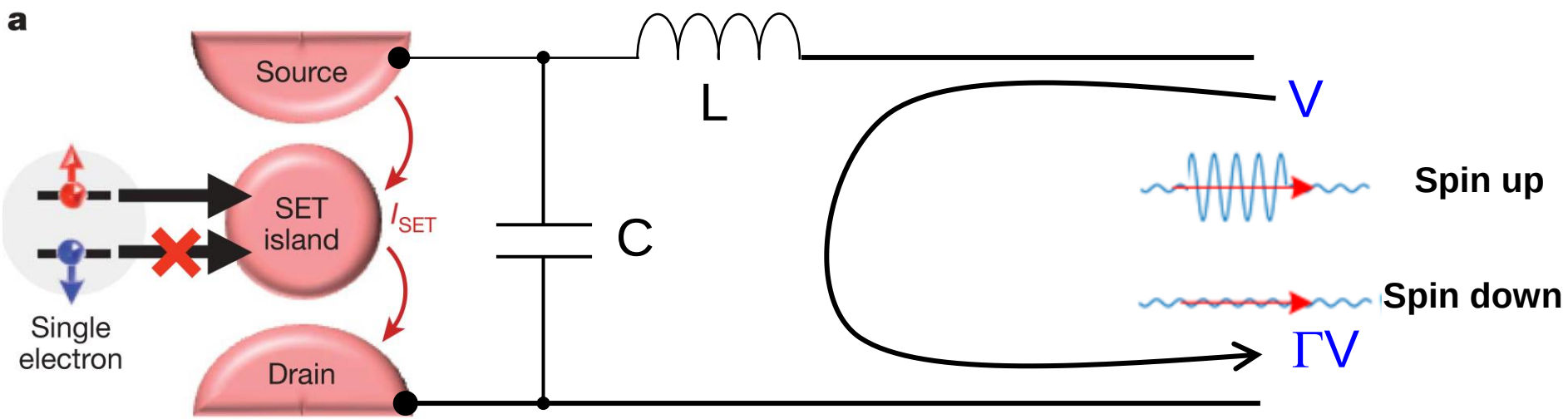
Matching network



SET resistance depends by the donor charge

Passive network to match the high resistance of the SET to the Z_0=50Ω of the line

Matching network

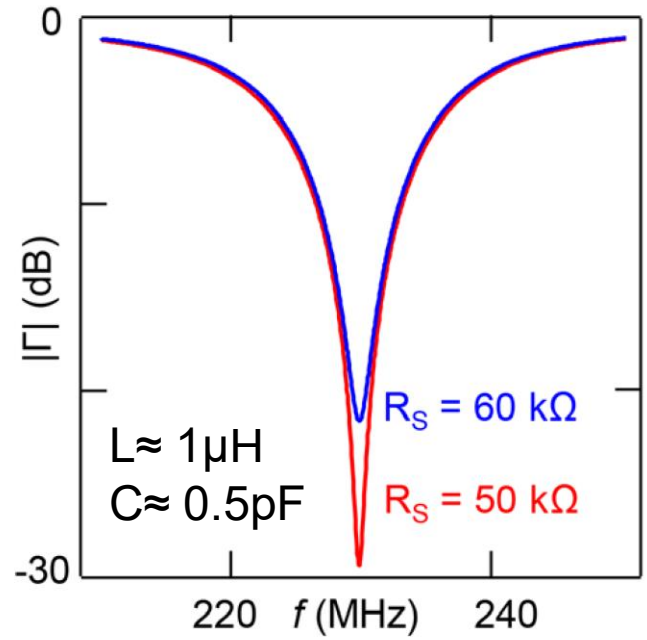


$$Z_L = R_{SET}\frac{1+\frac{sL}{R_{SET}}+s^2LC}{1+sCR_{SET}}$$

$$\omega_{res} = \frac{1}{\sqrt{LC}}$$

$$Z_L(\omega_{res}) = \frac{L}{CR_{SET}}$$

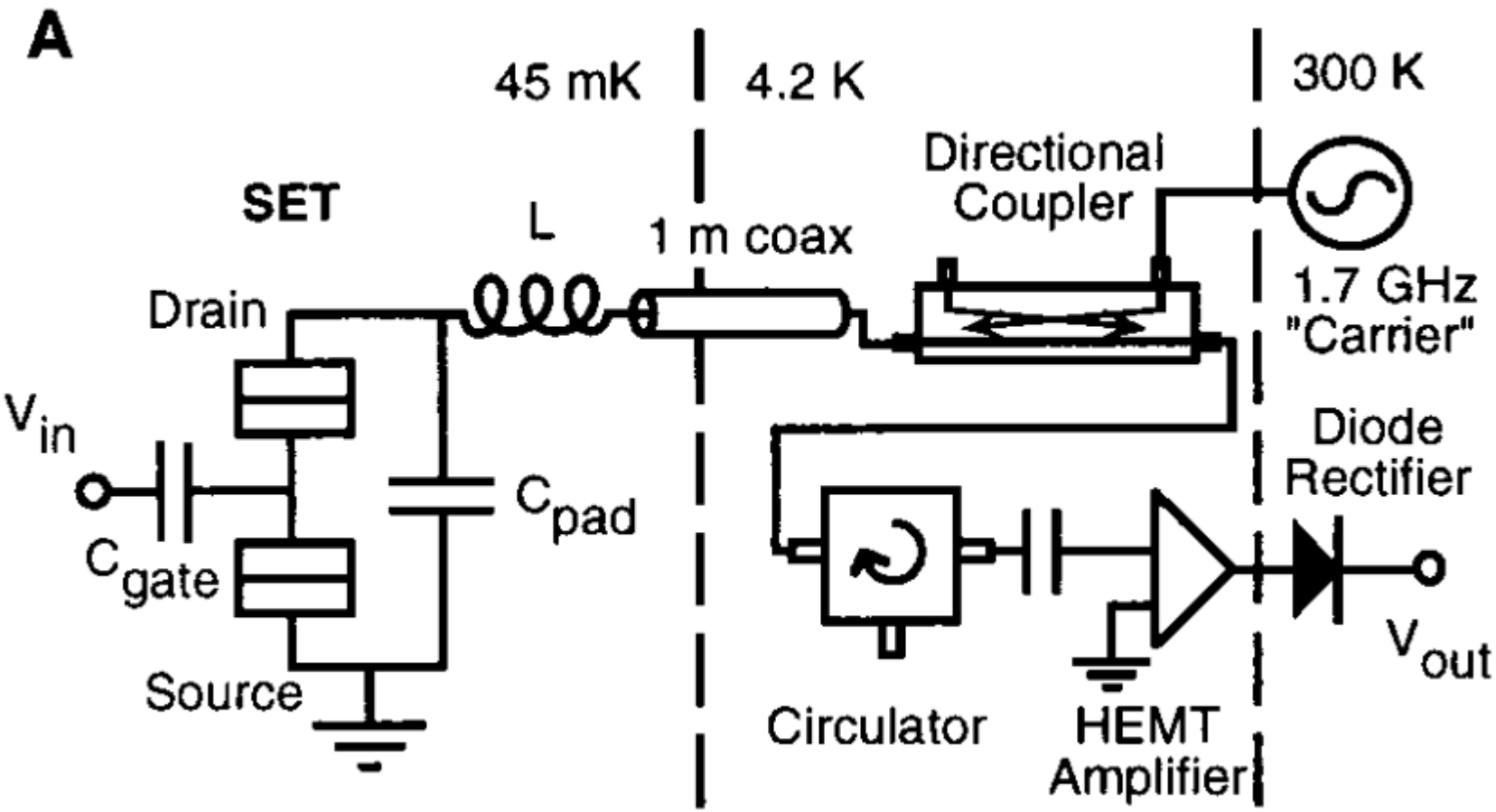
L,C selected to have $Z_L(\omega_{res}) \approx Z_0$



F. Vigneau, et al. *Appl. Phys. Rev.* (2023), doi: 10.1063/5.0088229.

Readout based on RF reflectometry

R. Schoelkopf, et al. “The radio-frequency single-electron transistor (RF-SET): A fast and ultrasensitive electrometer,” *Science*, vol. 280, no. 5367, pp. 1238–42, May 1998



Reflectometry allows high-sensitivity measurements despite long cables

(similar technique could be applied to the gate of the SET)

Recent review paper: F. Vigneau, et al. *Appl. Phys. Rev.* (2023), doi: 10.1063/5.0088229.

Quantum computer: wiring!

MIT Technology Review

Intelligent Machines

We'd have more quantum computers if it weren't so hard to find the damn cables

by Martin Giles, January 17, 2019

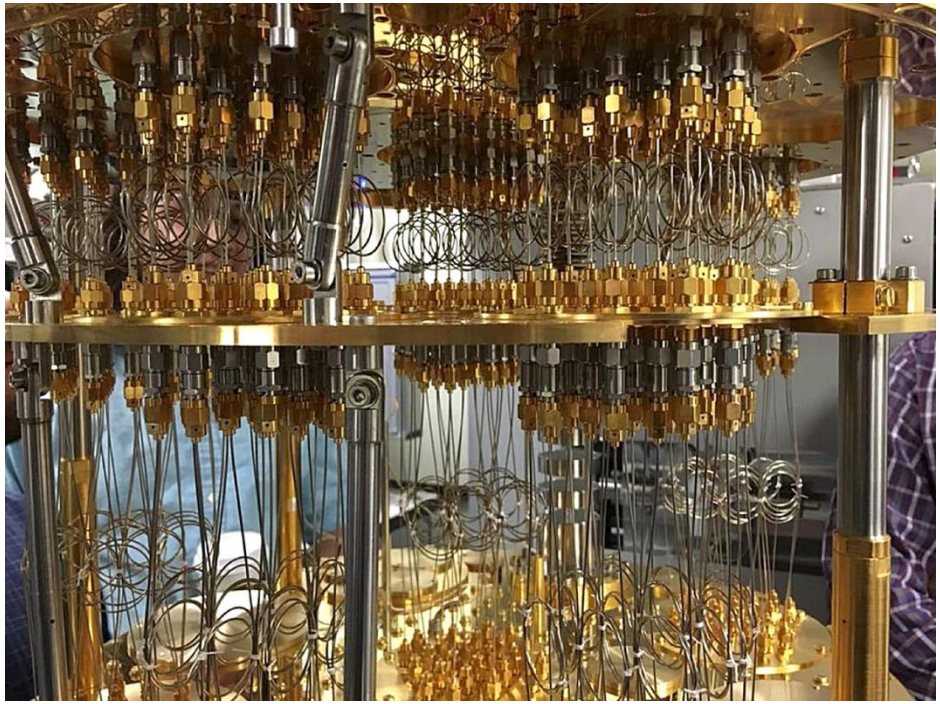
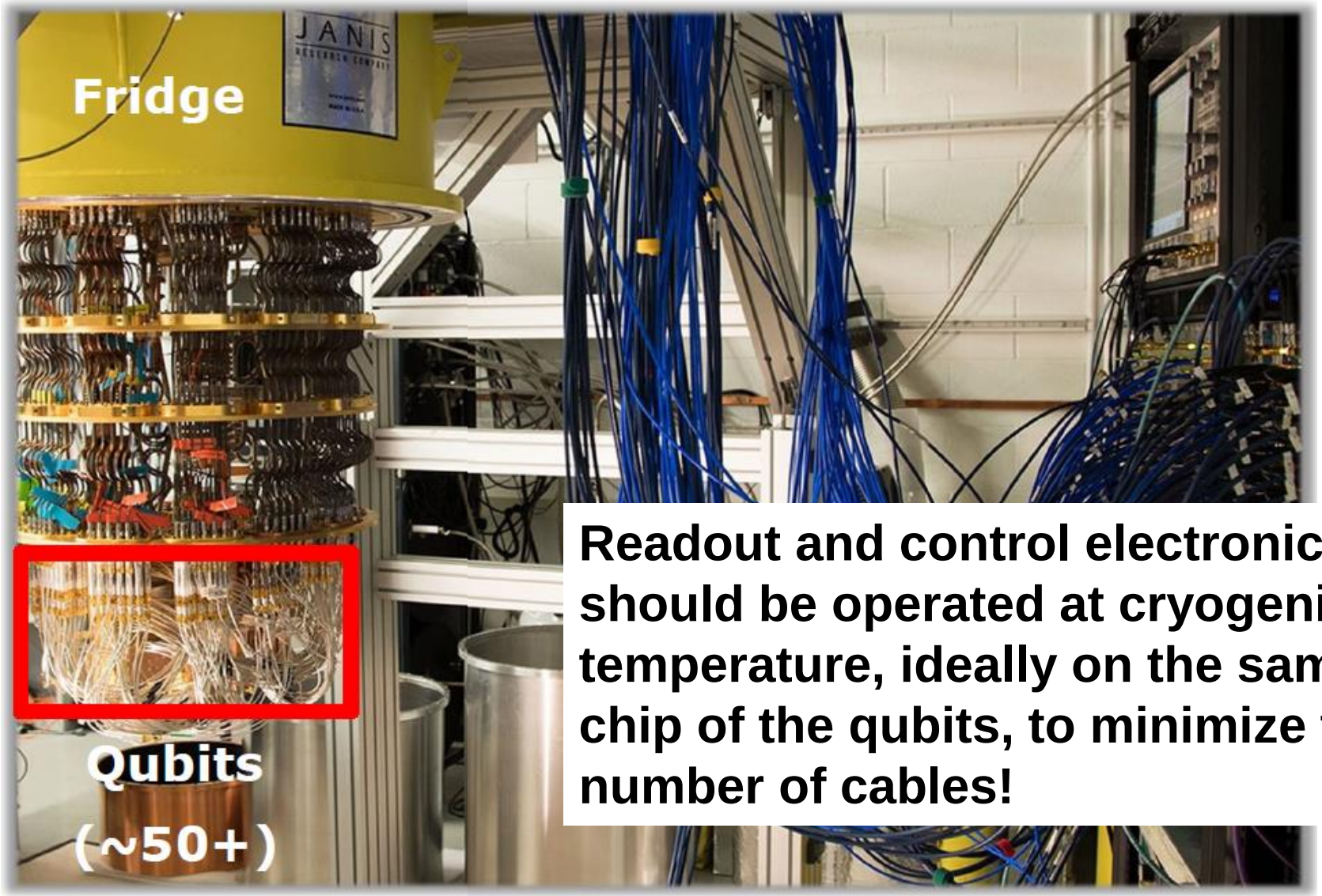


Image: IBM Research

Cables connecting qubits (<4K) to room temperature electronics are a limiting factor!

(≈ 2 coaxial cables /qubit)

Quantum computer: cryogenic electronics!



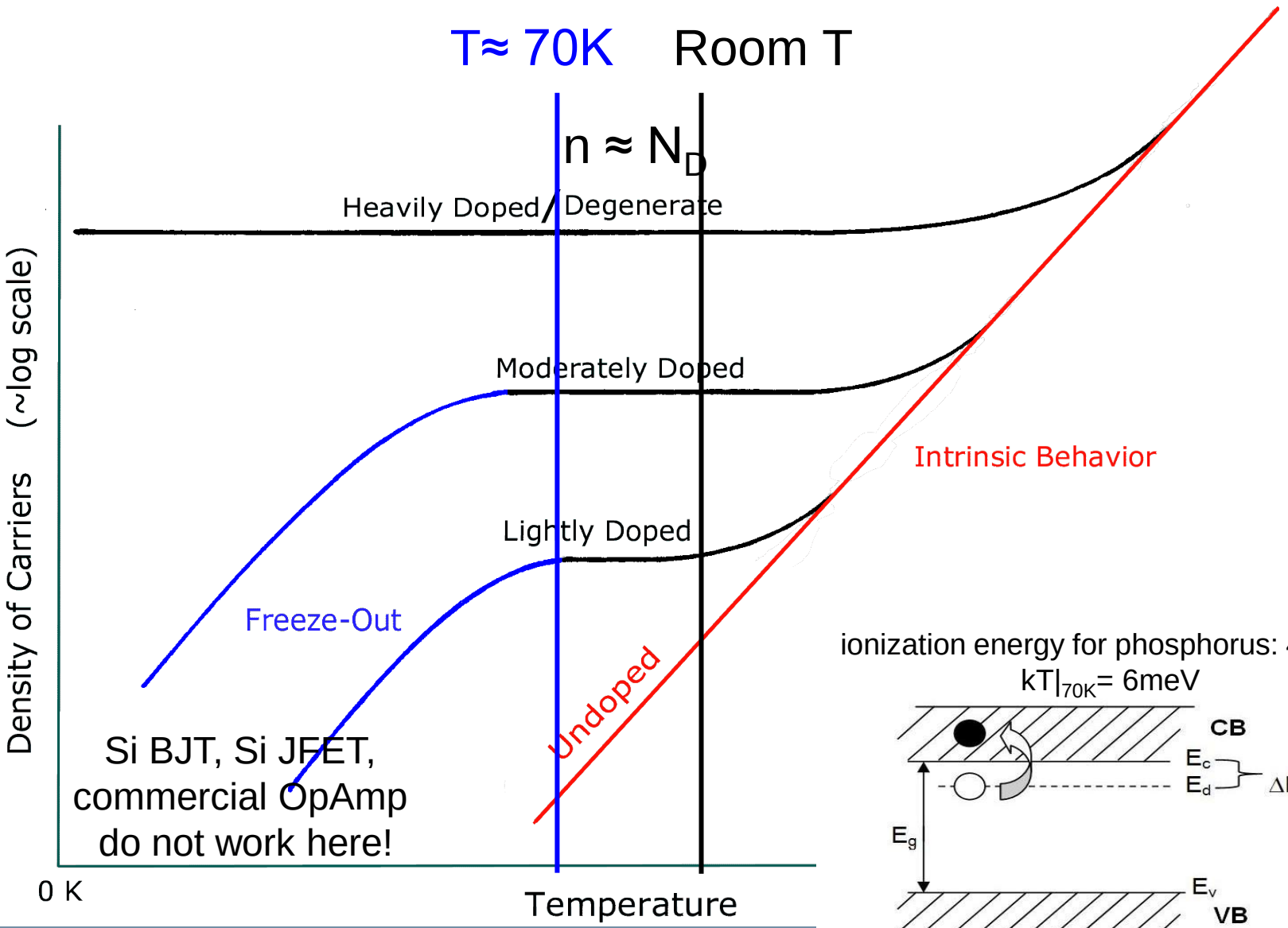
Readout and control electronics should be operated at cryogenic temperature, ideally on the same chip of the qubits, to minimize the number of cables!

[Bardin, ISSCC 2019]

Outline

- Spin detection using room temperature instrumentation
- Cryogenic electronics
  - Challenges
  - Design rules
- Examples

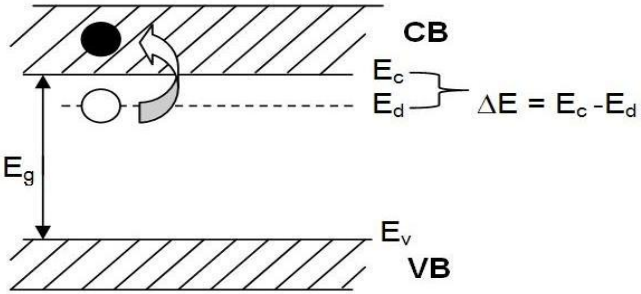
Freeze-out and degenerate semiconductor



http://www.extremetemperatureelectronics.com

ionization energy for phosphorus: 45meV

$kT|_{70K}$= 6meV



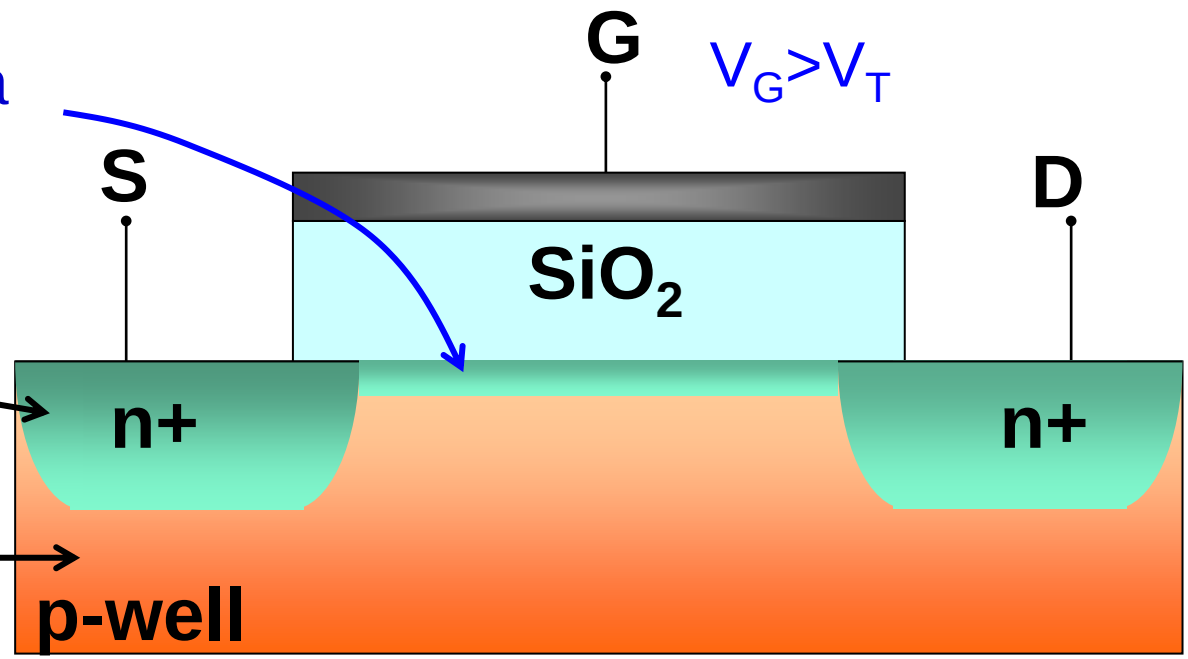
http://fog.ccsf.cc.ca.us/~wkaufmyn/

Electronics below the freeze-out temp.

electric field creates a conductive channel!

no freeze-out: conductive

freeze-out: insulator



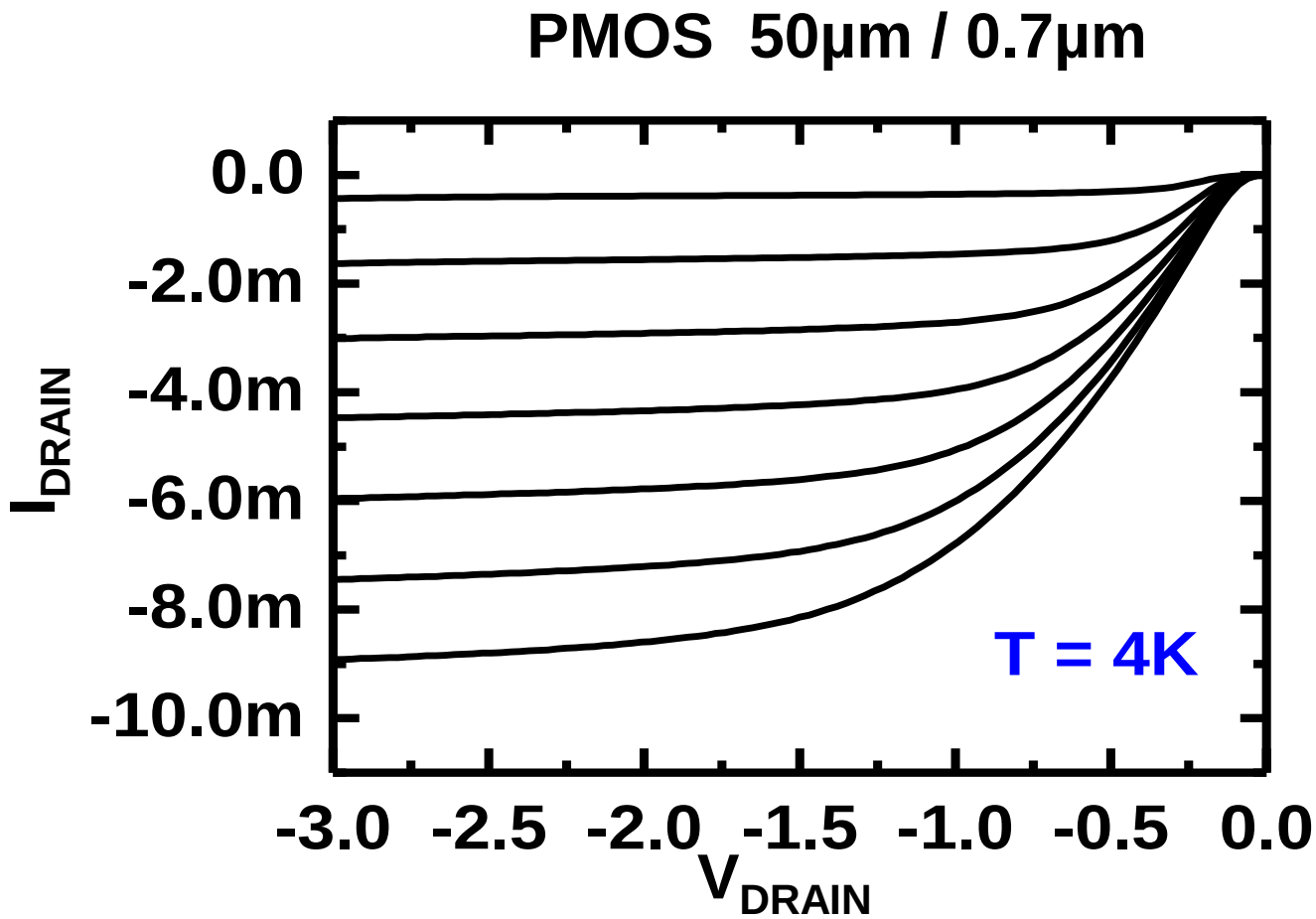
Silicon (standard) MOSFET operates below 40K!

Many GaAs devices operate at cryogenic temperature: degenerate at 10^{16} cm^{-3}

Limitation: small (and expensive) scale integration

MOSFET operating at 4K

Standard analog CMOS Technology 3.3V, 0.35µm

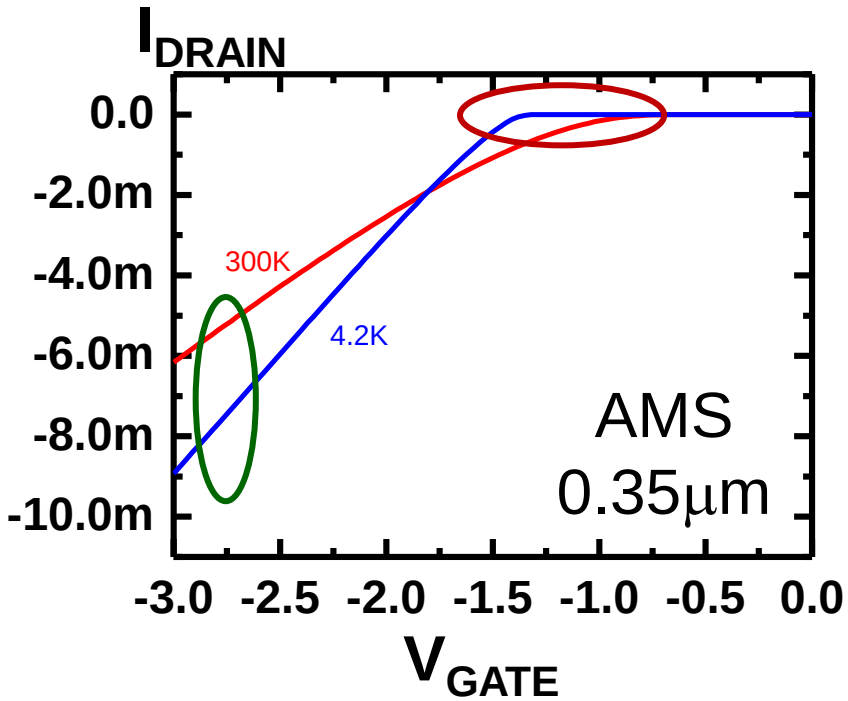


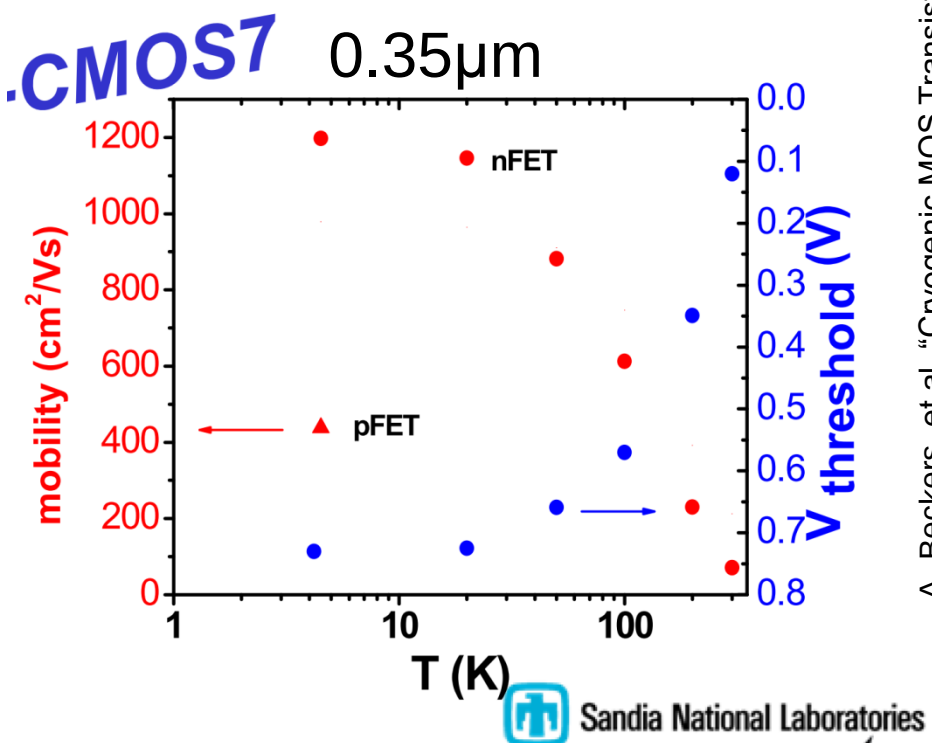
very similar to the room temperature behavior!

Effects of low temperature

- reduction in electron - phonon scattering
  → increase in carrier mobility

- substrate Fermi level shifts near to E_C (pMOS)
  → increase of the threshold voltage





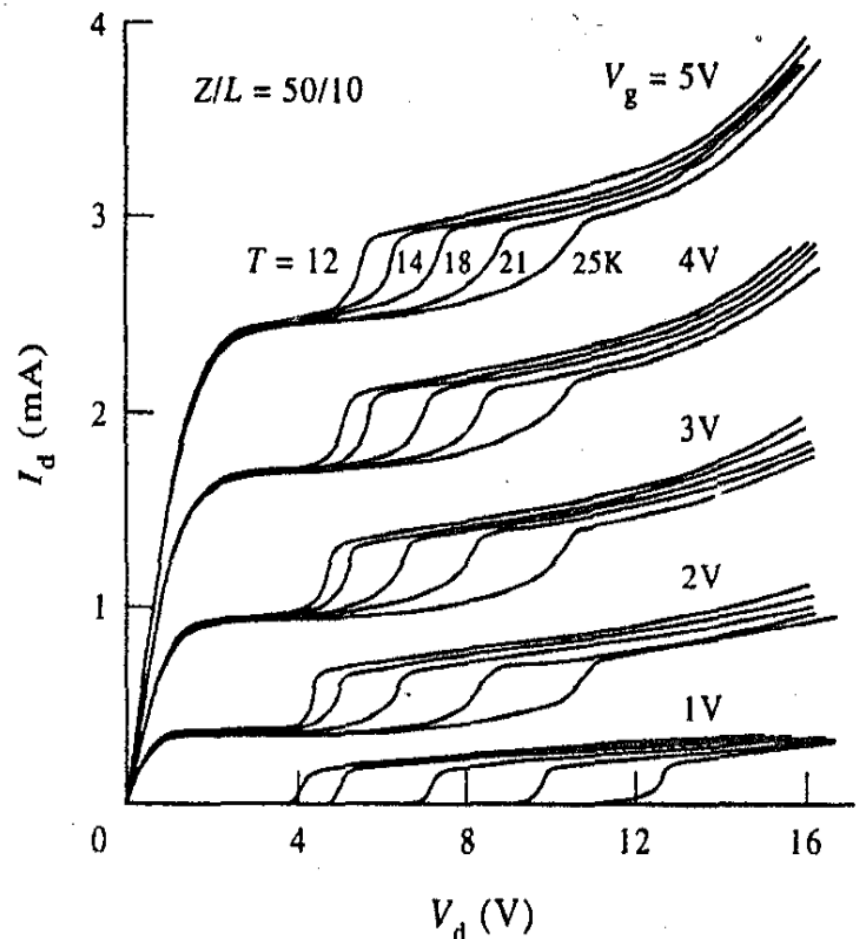
A. Beckers, et al. "Cryogenic MOS Transistor Model," *IEEE TED*, 2018.

Sandia National Laboratories

Eng et al. Silicon Qubit Workshop '09

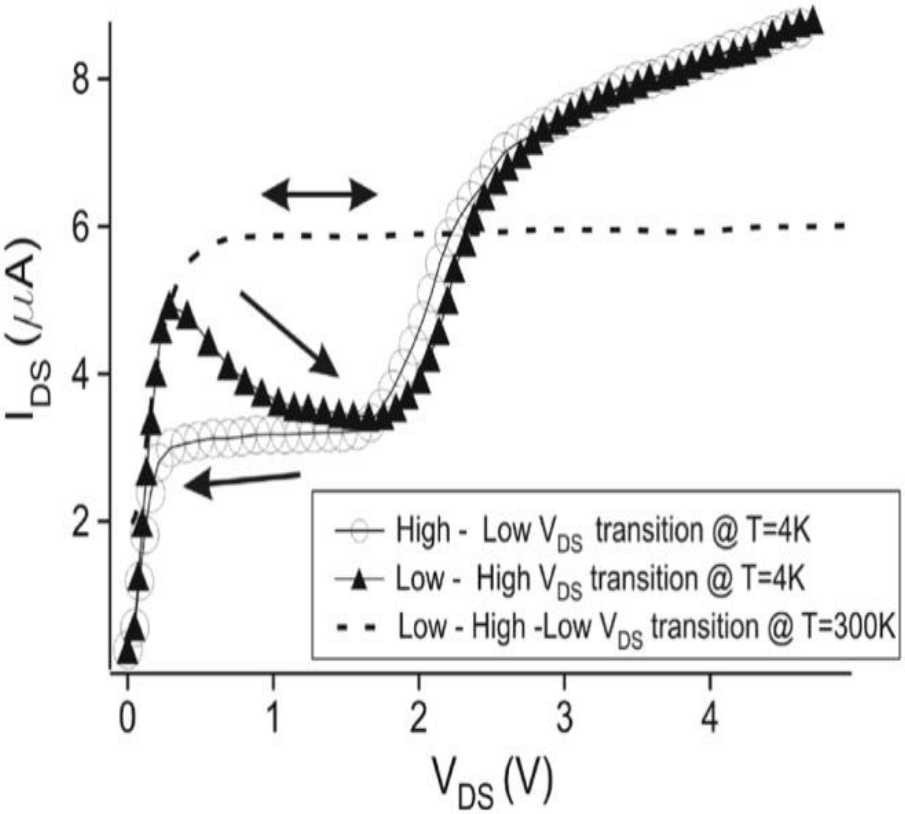
MOSFET operating at 4K: problems

kink effect



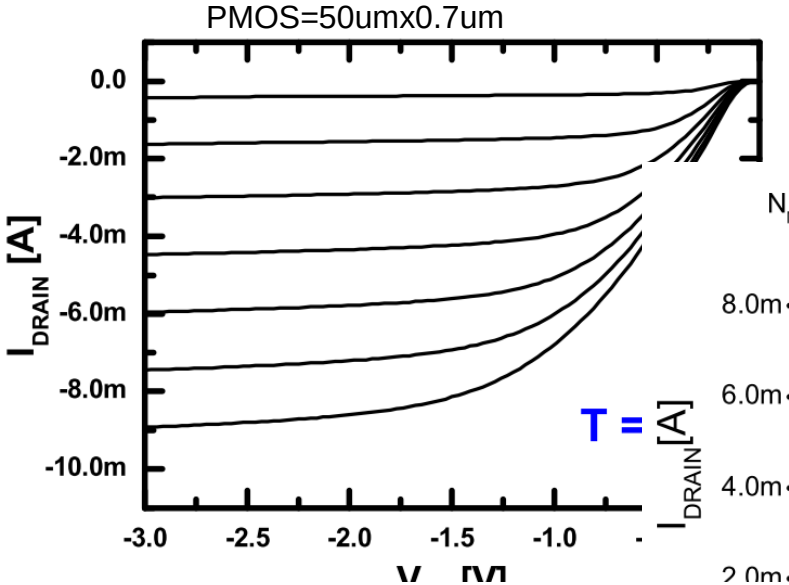
Ghibaudo, Balestra, "Low Temperature characterization of Silicon CMOS Devices", 1995

hyteresys

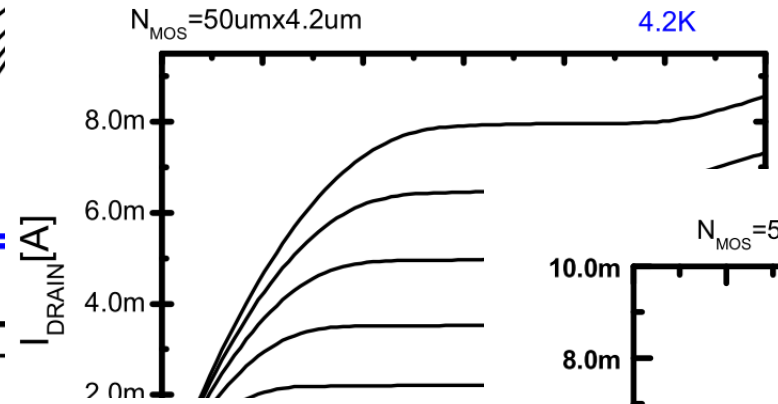


Y. Creten et al., IEEE J. Solid-State circuits, p. 2019 (2009)

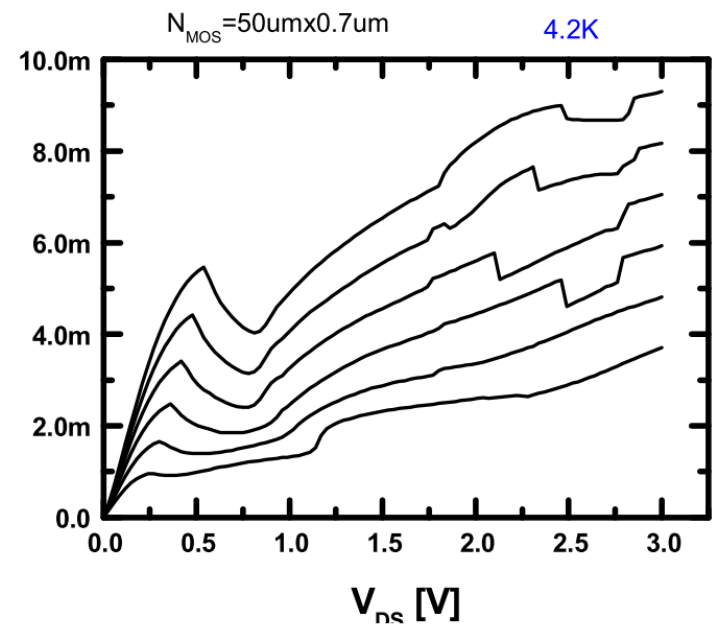
Problems are tech and size dependent

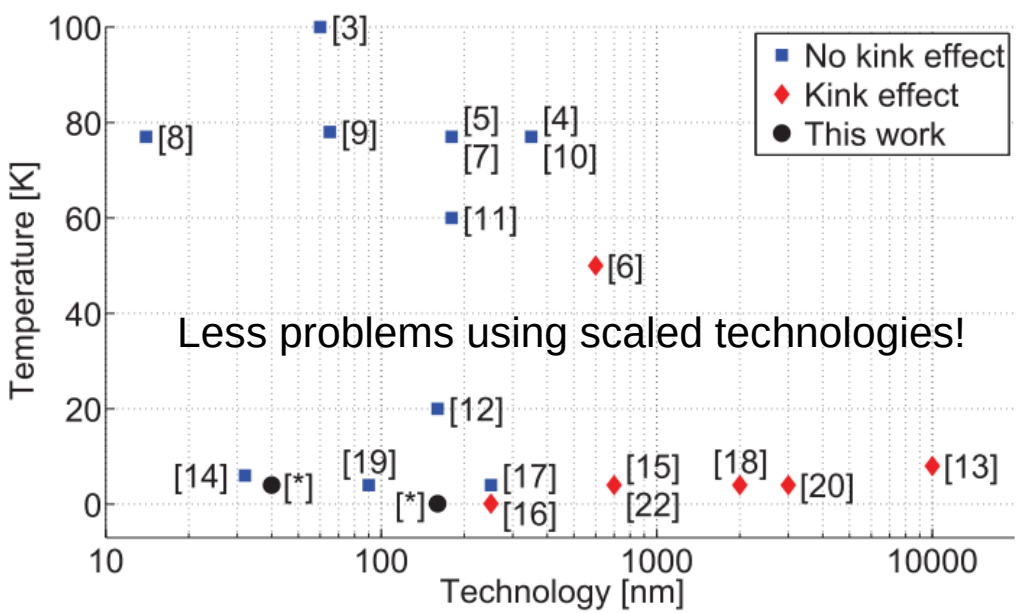


…and no models from the CMOS foundry!



AMS 0.35µm



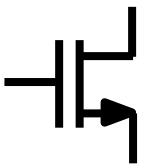


Less problems using scaled technologies!

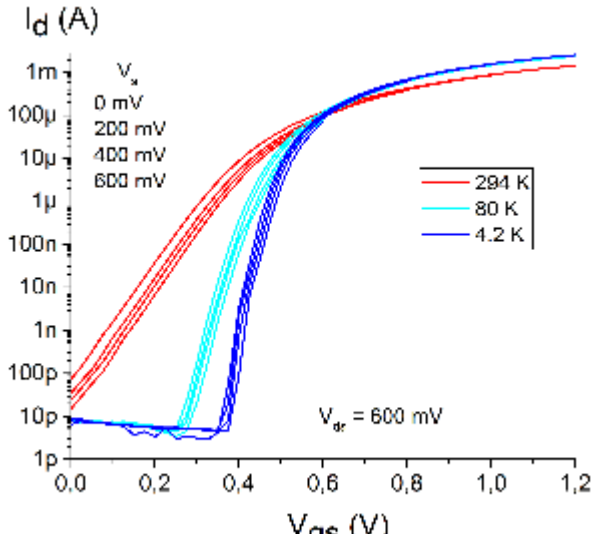
R. M. Incandela, et al.,pp. 58–61, 2017 ESSDERC.

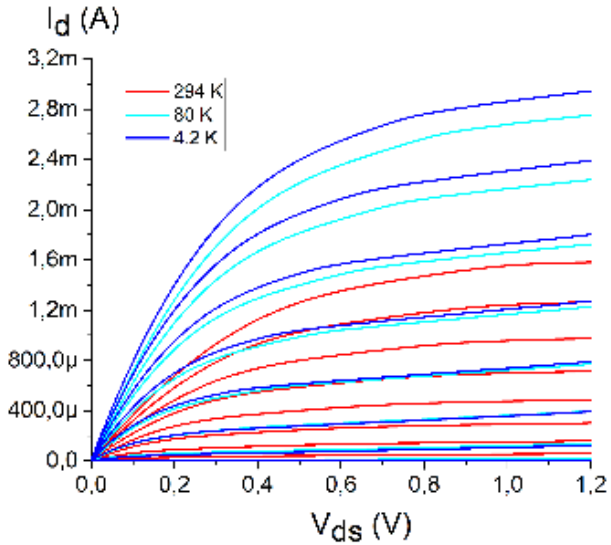
Quantum effects in small size MOSFETs!

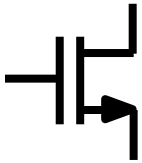
110nm CMOS



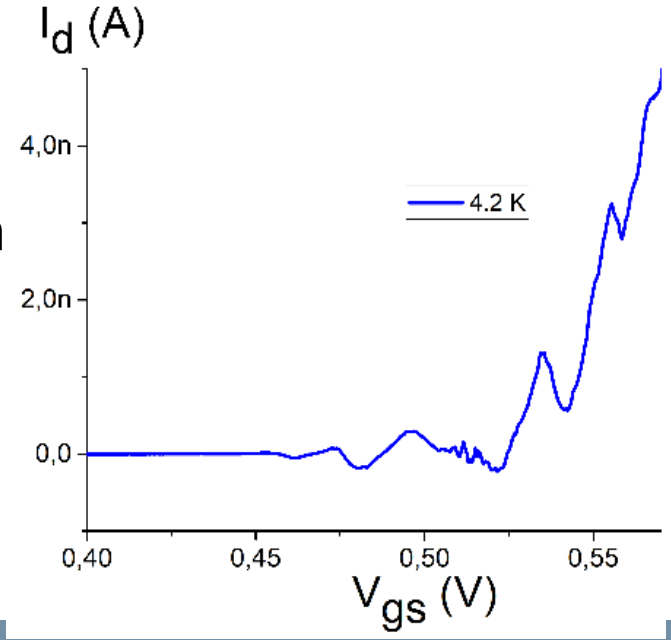
$$\frac{W}{L} = \frac{10\mu m}{0.5\mu m}$$

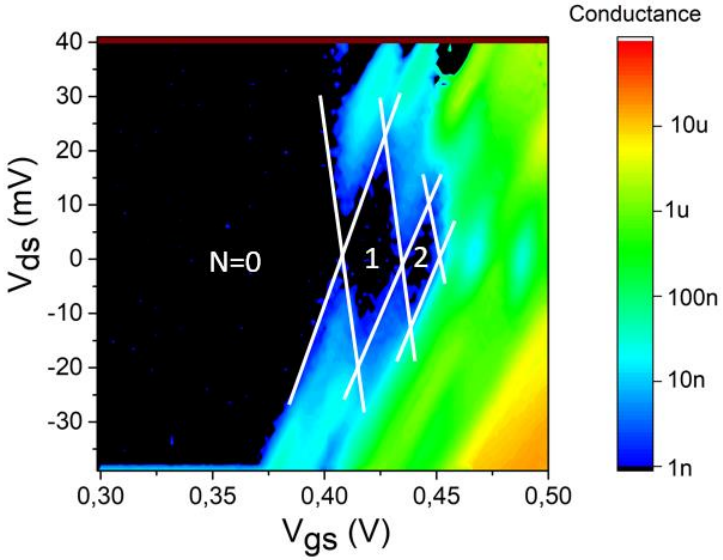






$$\frac{W}{L} = \frac{0.14\mu m}{0.1\mu m}$$





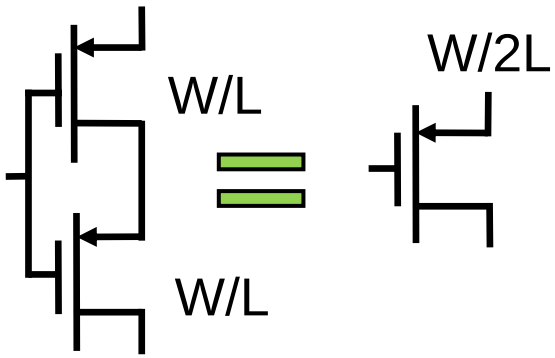
Design rule 1: characterize the technology!

MOS parameters strongly depend on the size and tech

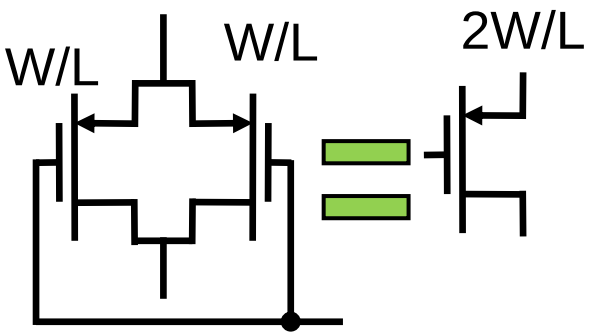
Experimental characterization of YOUR technology is MANDATORY

For simple circuits 1 nMOS and 1 pMOS is enough

series or parallel combinations of these basic transistors

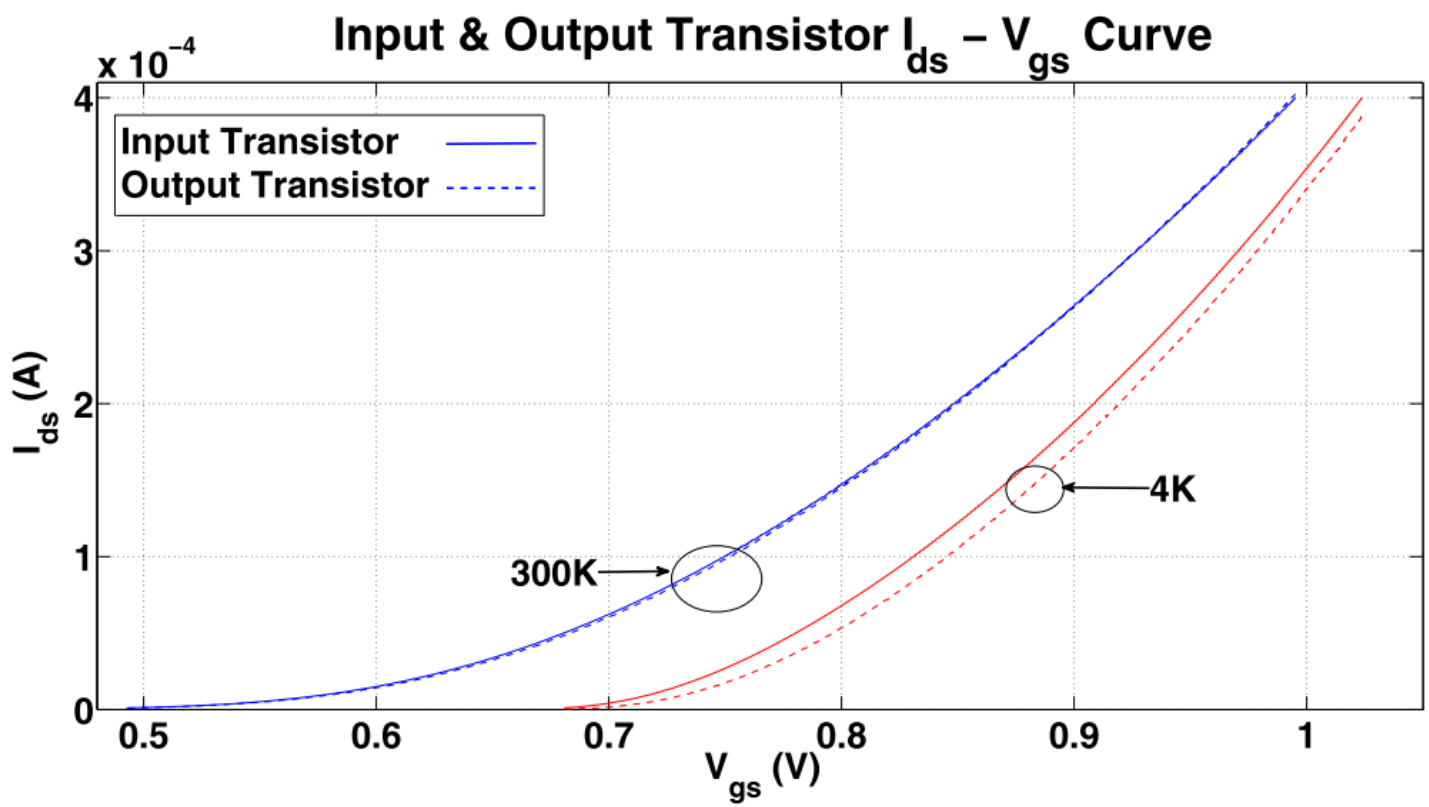


less conductive MOS



more conductive MOS

Design rule 2: pay attention to mismatch!

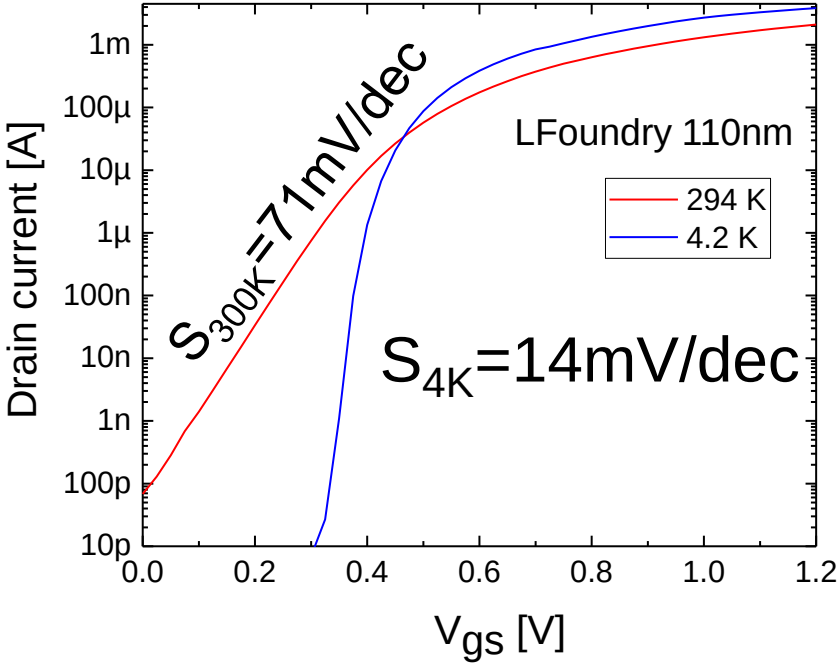


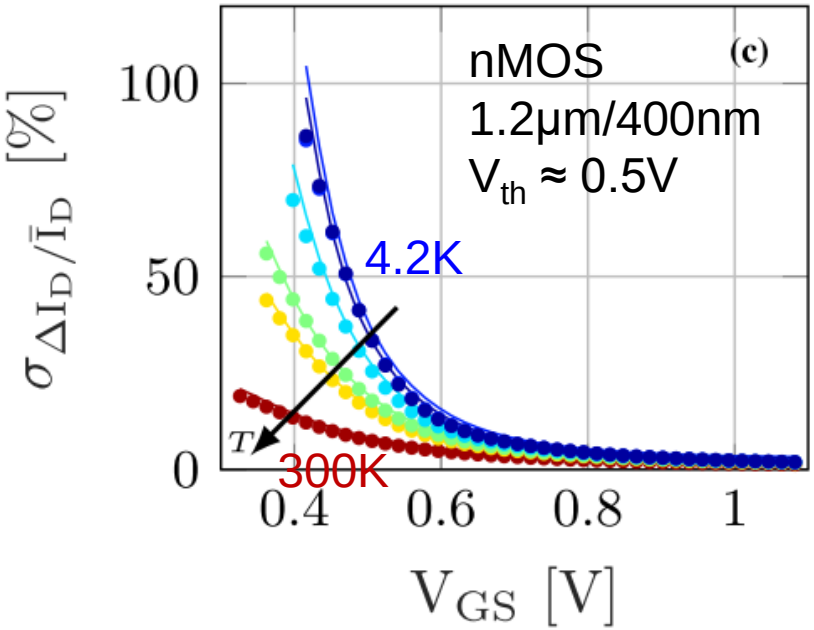
K. Das et al. EEE Symposium on Circuits and Systems, 2010

worsening of mismatch by a factor of 1.5-3 at low temperature compared to room temperature (tech dependent).

➡ Degradation of the offset voltage, linearity of ADC, DAC, bias setting

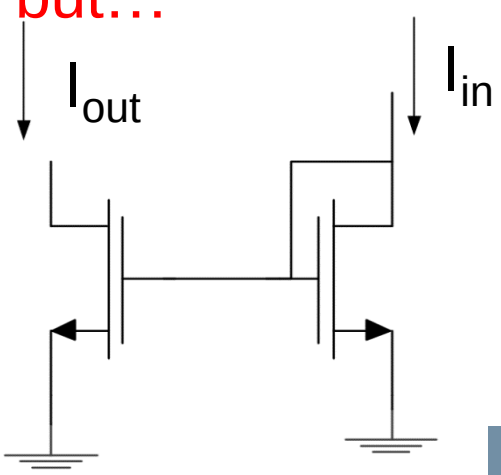
Design rule 3: subthreshold is critical





P. A. T'Hart, et al. *IEEE J. Electron Devices Soc.*, pp. 263–273, 2020

Higher g_m and I_{on}/I_{off}, good!
but…



V_T mismatch of 5mV:

$$I_{out,300K} \approx I_{in}\, 10^{\frac{5mV}{S_{300K}}} = I_{in} \cdot 1.17$$

$$I_{out,4K} \approx I_{in}\, 10^{\frac{5mV}{S_{4K}}} = I_{in} \cdot 2.28$$

Design rule 4: dynamic range

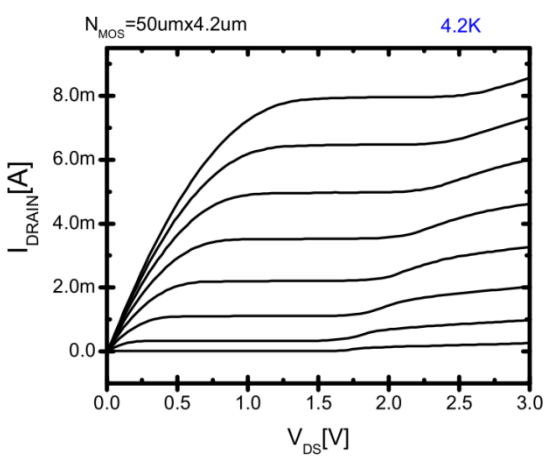
AMS 0.35µm

- $V_{T,n}$ from 0.45V to 0.7V
- $V_{T,p}$ from -0.7V to -1.4V
- Power supply: 3.3V
- no subthreshold

stack up few transistors!

and

kink effect



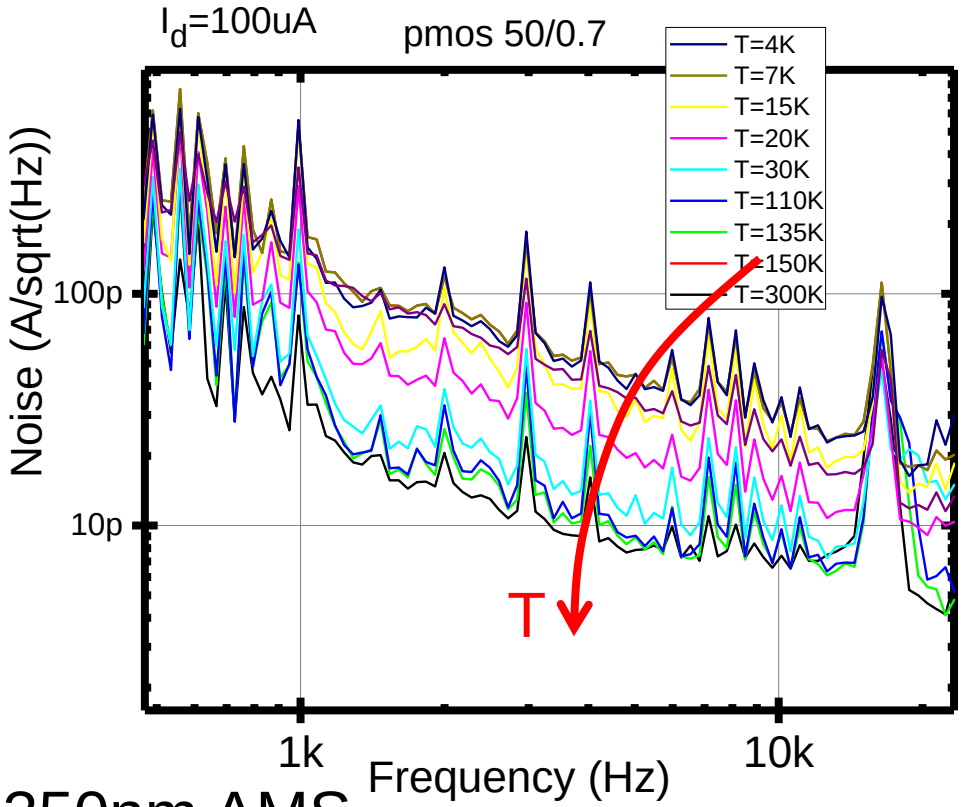
limit the V_{DS}!

Noise

Thermal noise: $\overline{e_n^2} = 4kT\dfrac{\gamma}{g_m}$

T ↘ , g_m ↗ → ***noise ↘↘***
(0.1nV/ √Hz))

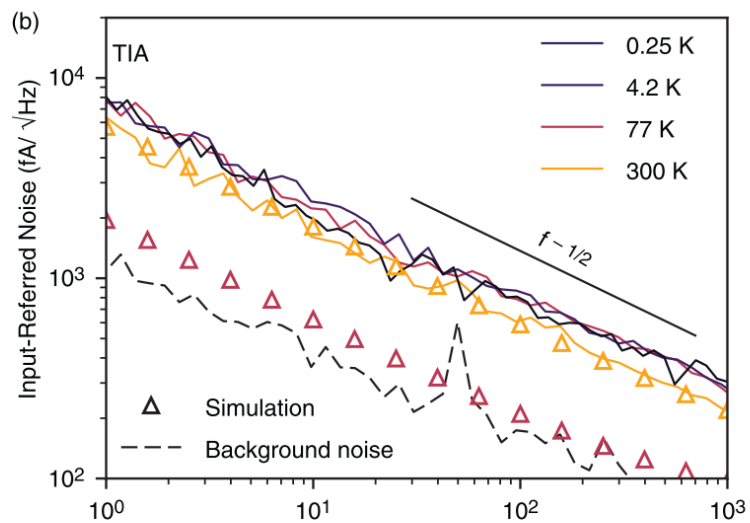
Flicker noise: increase or independent (tech and size dependent)



350nm AMS

dominant noise up to tens of MHz

28nm FDSOI tech.



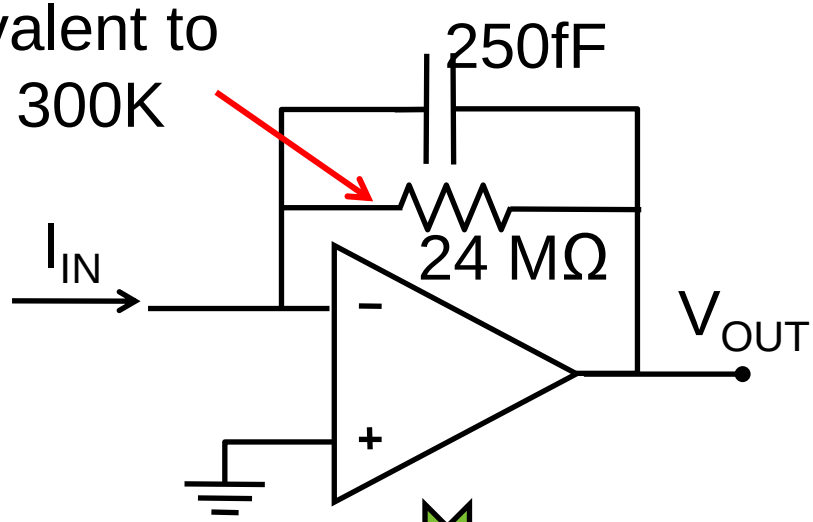
L. Le Guevel *et al.*, "Low-power transimpedance amplifier for cryogenic integration with quantum devices," *Appl. Phys. Rev.*, 2020

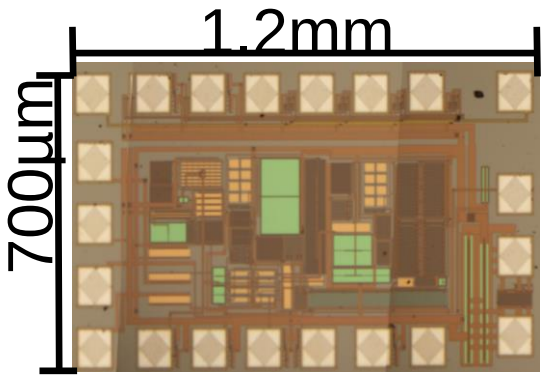
Outline

- Spin detection using room temperature instrumentation
- Cryogenic electronics
  - Challenges
  - Design rules
- Examples

Cryogenic transimpedance amplifier

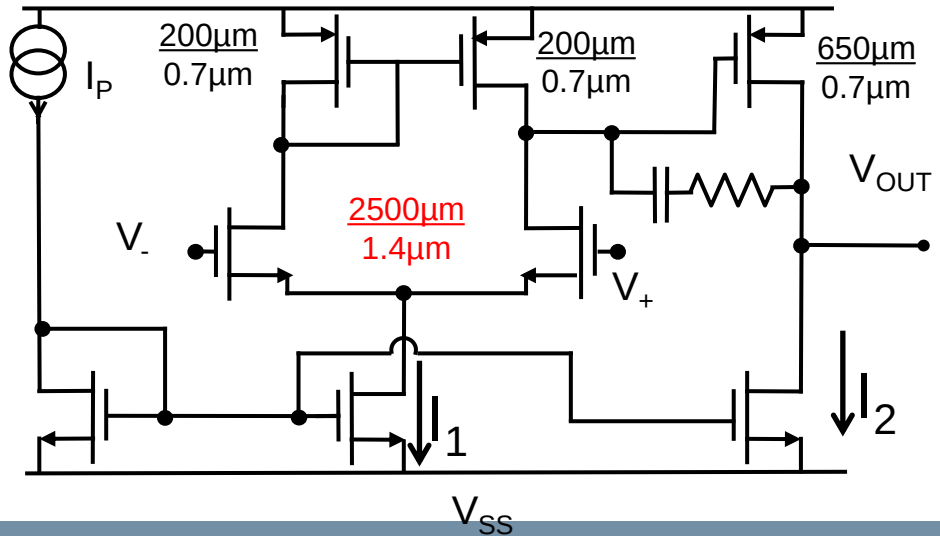
Noise equivalent to
1.7GΩ @ 300K





CMOS Technology
3.3V 0.35µm

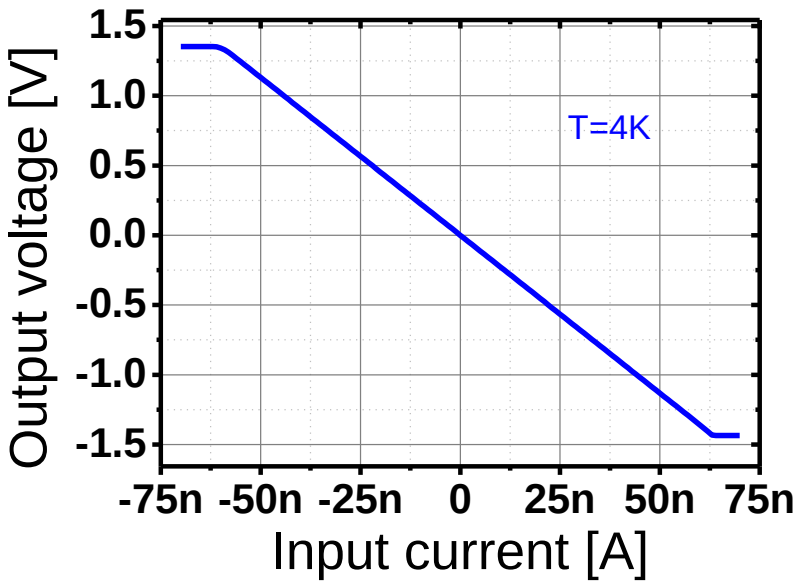
nMos: 50µm/1.4µm
pMos: 50µm/0.7µm



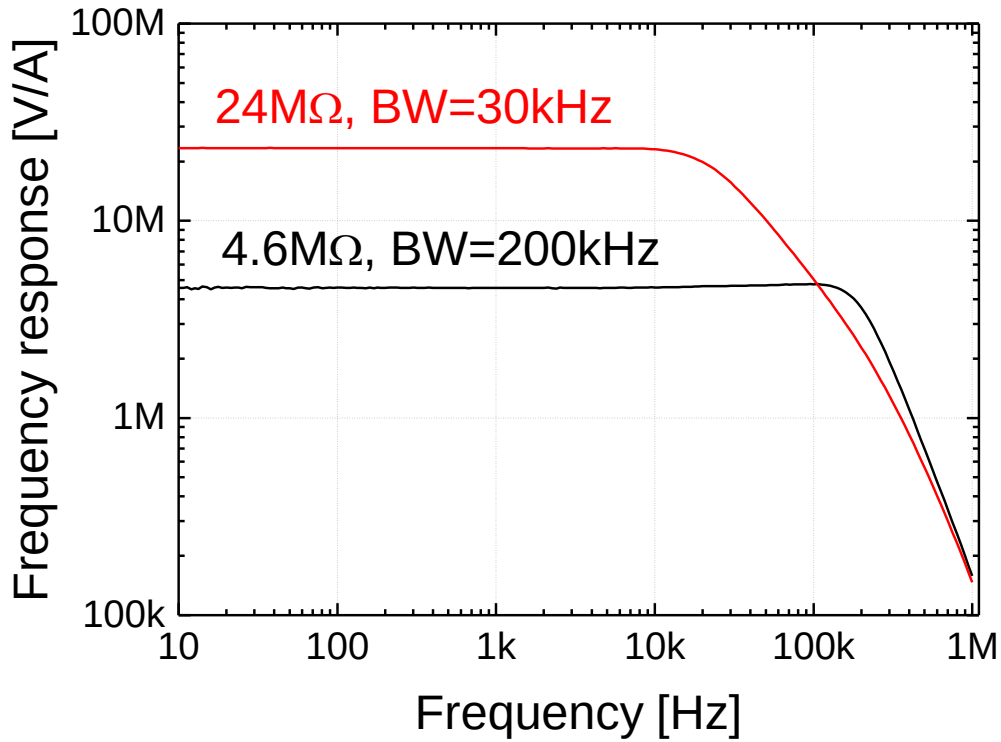
(simplified scheme)

F. Guagliardo et al., in "*Single Atom Nanoelectronics*", ed. E. Prati and T. Shinada, Pan Stanford Publishing (2013)

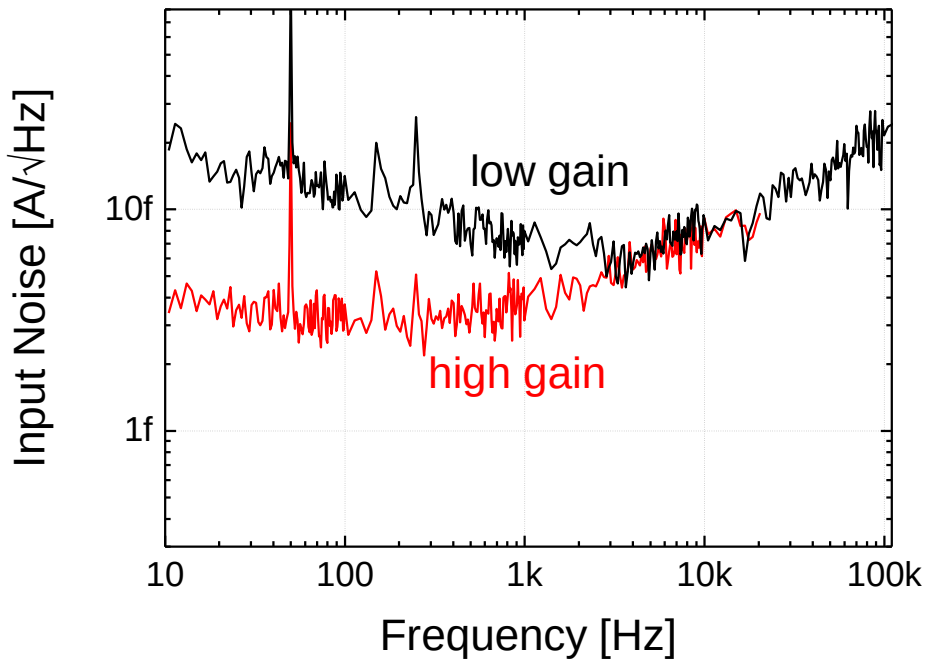
Measurements at 4 Kelvin



Gain, linearity and bandwidth match the simulations



Measurements at 4 Kelvin

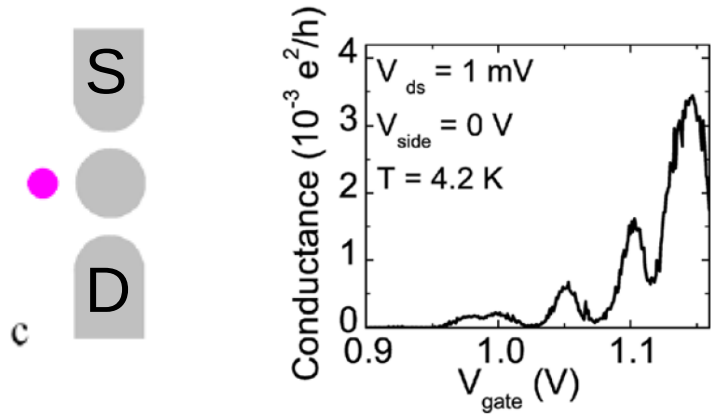


- 2.3 pA_{RMS} resolution (14 pA)
- 32 kHz Bandwidth (190 kHz)

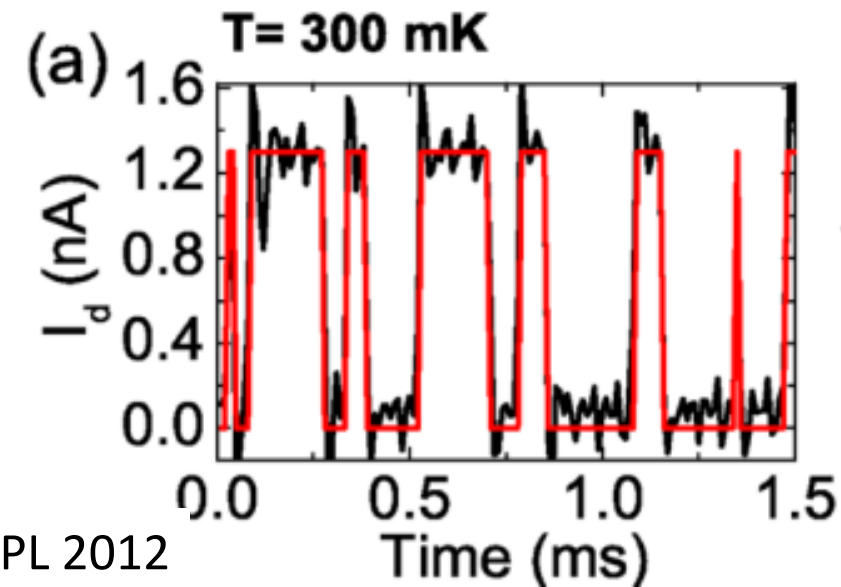
  ≈ 30 times better of RT

M. L. V. Tagliaferri et al, *IEEE Trans. Instrum. Meas.*, pp. 1827–1835, Aug. 2016.

Quantum dots with a single ion implanted

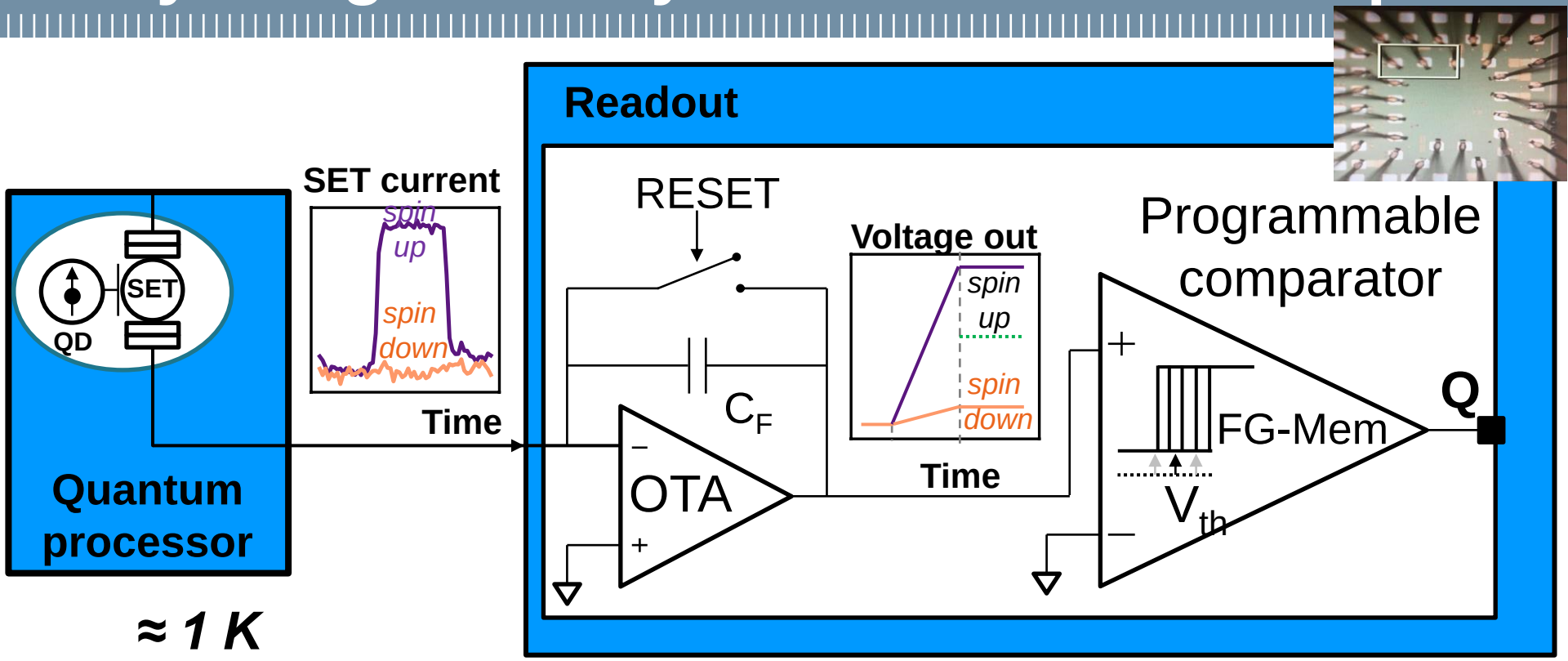


Single charge state sensing



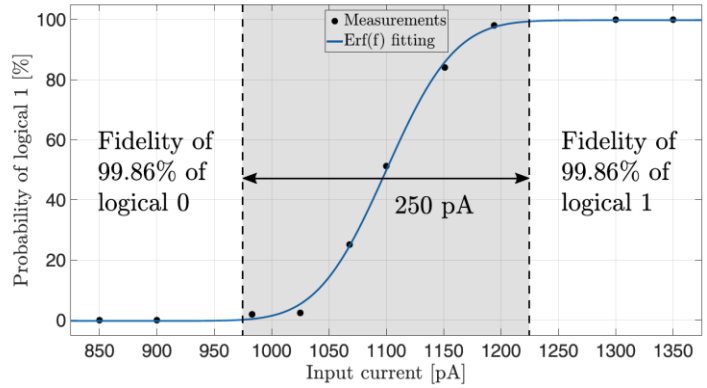
Mazzeo et al APL 2012

Fully-integrated Cryo-CMOS readout of qubits

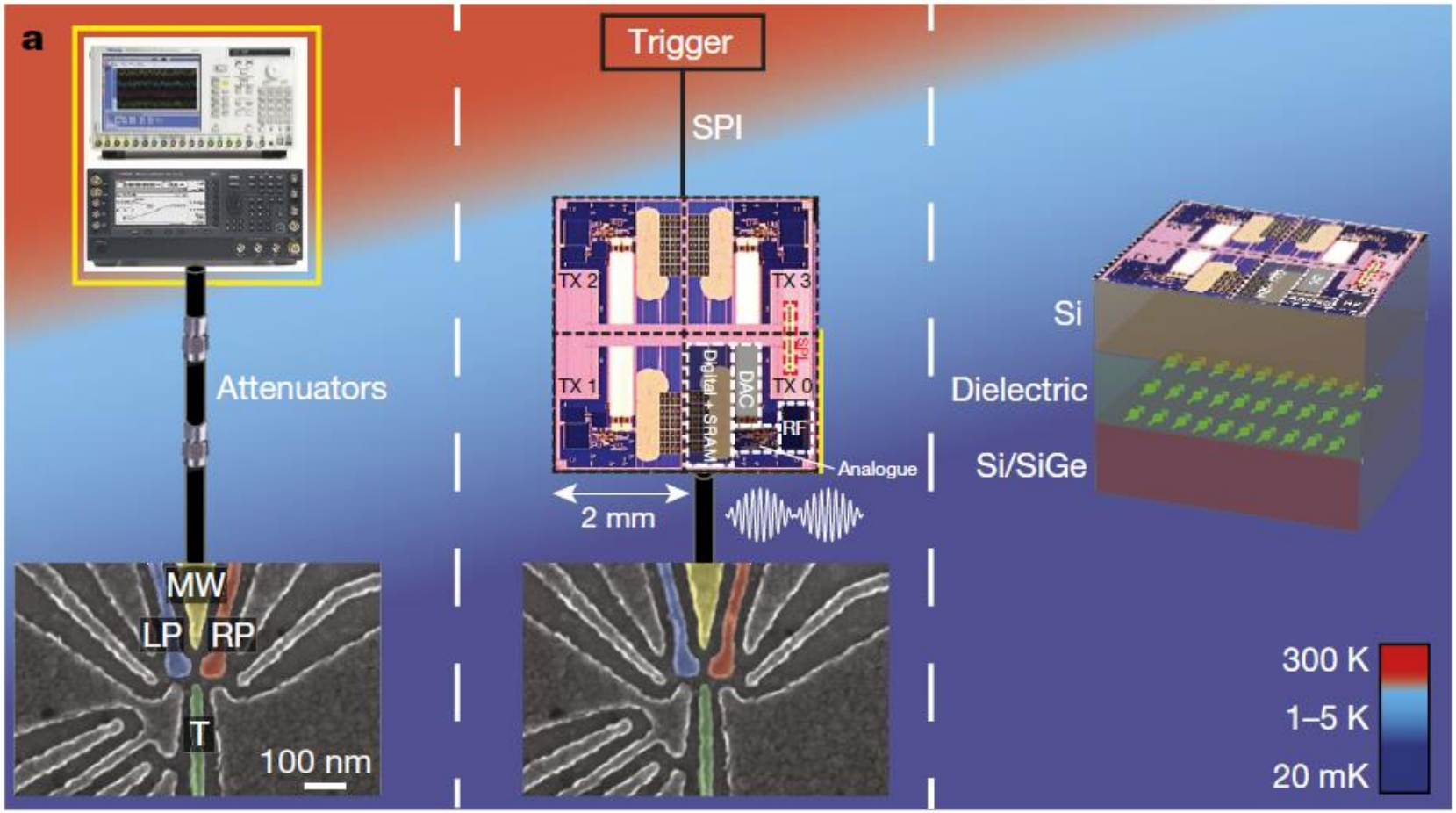


validated @ 4.2 K

- Direct current readout at 4.2K
- Readout in 500ns
- Power consumption = 1.2mW
- Area < 1 mm^2
- Unconventional use of floating gates for a compact, programmable, and precise comparator (<1mV)



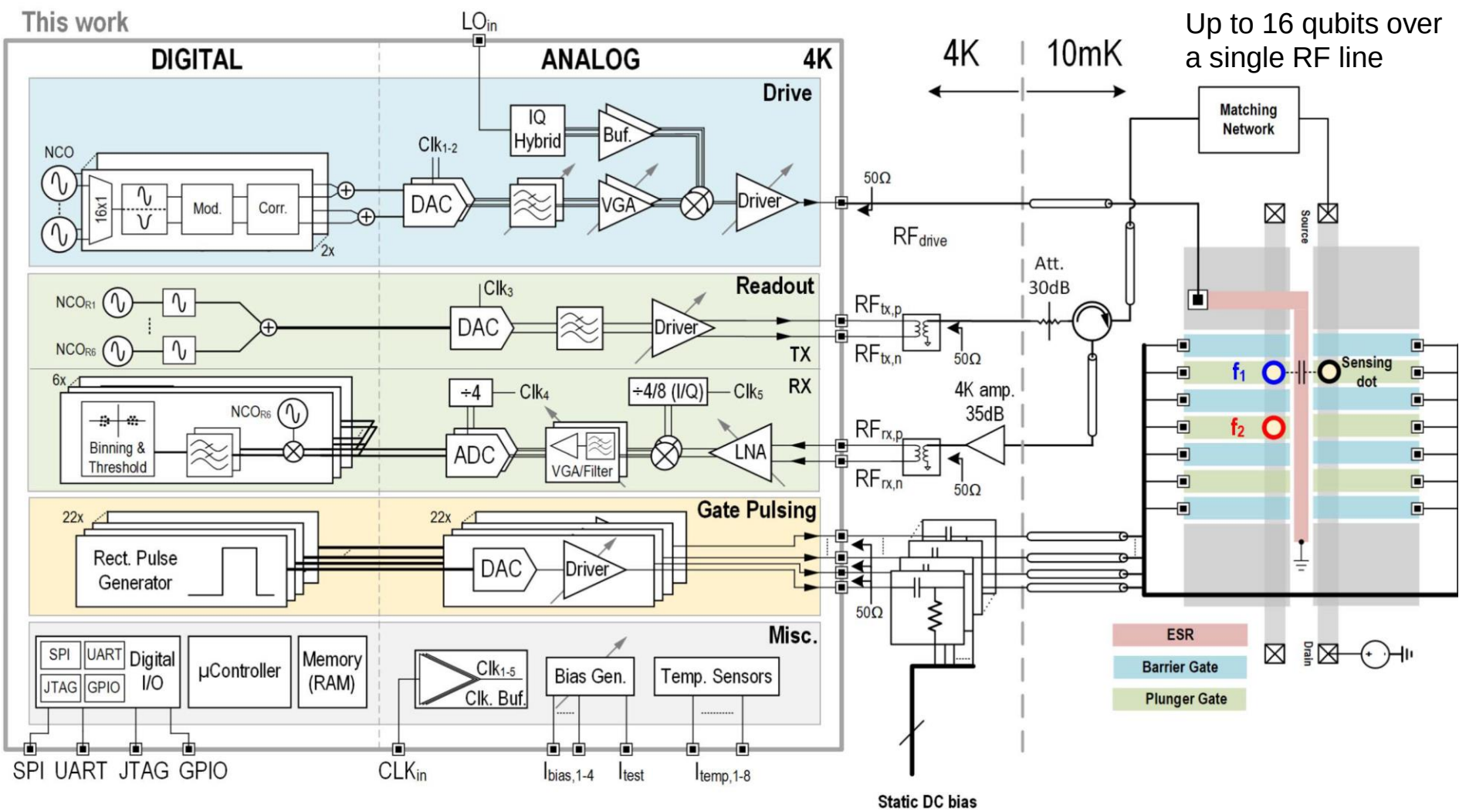
Cryogenic quantum controller



Today Tomorrow Future

X. Xue *et al.*, “CMOS-based cryogenic control of silicon quantum circuits,” *Nature*, pp. 205–210, 2021

Intel quantum controller for spin qubits



J. Park, et al. ,“A Fully Integrated Cryo-CMOS SoC for State Manipulation, Readout, and High-Speed Gate Pulsing of Spin Qubits,” *IEEE J. Solid-State Circuits*, vol. 56, no. 11, pp. 3289–3306, 2021

Thank you for you attention!